

# SERVICE MANUAL

**TS-440S** PS-50, PS-430, SP-430, MB-430, VS-1  
AT-440, YK-88C/CN, YK-88S/SN

## HF TRANCEIVER



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## SPECIFICATIONS

### (GENERAL)

**Transmitter frequency range:**

160m BAND 1.8 ~ 2.0MHz  
 80m BAND 3.5 ~ 4.0MHz  
 40m BAND 7.0 ~ 7.3MHz  
 30m BAND 10.1 ~ 10.15MHz  
 20m BAND 14.0 ~ 14.35MHz  
 17m BAND 18.068 ~ 18.168MHz  
 15m BAND 21.0 ~ 21.45MHz  
 12m BAND 24.89 ~ 24.99MHz  
 10m BAND 28.0 ~ 29.7MHz

**Receive frequency range:**

100kHz ~ 30MHz

**Mode:**

A1(CW), A3J(SSB), A3(AM), F1(FSK), F3(FM)

**Antenna impedance:**

50 Ohm (TX: 20 ~ 150 Ohm with AT)

**Power requirement:**

12.0 ~ 16.0V DC

**Power consumption:**

**RX no signal input:**

Approx. 1.9A

**TX:**

Approx. 20A

**Frequency configuration:**

**RX unit:**

1st IF 45.05MHz, 2nd IF 8.83MHz, 3rd IF 455kHz

**TX unit: (A1,A3J,A3,FSK)  
(F3)**

1st IF 455kHz, 2nd IF 8.83MHz, 3rd IF 45.05MHz

1st IF 36.22MHz, 2nd IF 45.05MHz

CW, SSB, AM, FSK, FM: Triple conversion superheterodyne

FM: Double conversion superheterodyne

**Semiconductors:**

	TS-440S	TS-440S (with AT)
Tr's	157	174
FET's	22	22
IC's	49	58
Diod's	257	277

**Dimensions:**

	TS-440S	TS-440S (with AT)
W(mm)	270 (279)	270 (279)
H(mm)	96 (108)	96 (108)
D(mm)	313 (335)	313 (335)
Weight(kg)	6.3	7.3

The numbers in the parenthesis include protections.

### (TRANSMITTER)

**Rated final power input:**

Band	Mode	A1, A3J, F1, F3	A3
	1.8 ~ 28 MHz		200 W PEP

**Carrier suppression:**

More than 40dB

**Unwanted sideband suppression:**

More than 50dB

**Harmonic content:**

Less than -40dB

**Transmit frequency character:**

400 ~ 2600Hz (-6dB)

**Maximum frequency deviation (FM):**

±5kHz

**Microphone impedance:**

500Ω ~ 50kΩ

## SPECIFICATIONS

### (RECEIVER)

#### Sensitivity:

Mode \ Freq.	100 ~ 150kHz	150 ~ 500kHz	0.5 ~ 1.6MHz	1.6 ~ 30MHz
SSB,CW,FSK (S/N10dB)	Less than 2.5 $\mu$ V (8dB $\mu$ )	Less than 1 $\mu$ V (0dB $\mu$ )	Less than 4 $\mu$ V (12dB $\mu$ )	Less than 0.25 $\mu$ V (-12dB $\mu$ )
AM (S/N10dB)	Less than 25 $\mu$ V (28dB $\mu$ )	Less than 13 $\mu$ V (22dB $\mu$ )	Less than 40 $\mu$ V (32dB $\mu$ )	Less than 2.5 $\mu$ V (8dB $\mu$ )
FM (12dB SINAD)	—	—	—	Less than 0.7 $\mu$ V (-3 dB $\mu$ )

#### Squelch sensitivity: (Threshold)

Mode \ Freq.	100 ~ 150kHz	150 ~ 500kHz	0.5 ~ 1.6MHz	1.6 ~ 30MHz
SSB,CW,AM,FSK	Less than 20 $\mu$ V (26dB $\mu$ )	Less than 10 $\mu$ V (20dB $\mu$ )	Less than 20 $\mu$ V (26dB $\mu$ )	Less than 2 $\mu$ V (6dB $\mu$ )
FM	—	—	—	Less than 0.32 $\mu$ V (-10dB $\mu$ )

#### Image ratio:

50dB or more (100kHz ~ 1.6MHz)  
70dB or more (1.6 ~ 30MHz)

#### IF rejection:

50dB or more (FM 3rd image ratio)  
50dB or more (100kHz ~ 1.6MHz)  
70dB or more (1.6MHz ~ 30MHz)

#### Selectivity:

Mode \ Freq.	-6dB	-60dB
SB,CW,FSK	More than 2kHz	Less than 4.4kHz
AM	More than 4kHz	Less than 18kHz (-50dB)
FM	More than 12kHz	Less than 25kHz (-50dB)

#### IF SHIFT variable range:

$\pm$ 0.9kHz or more

#### RIT/XIT variable range:

$\pm$ 1kHz or more

#### Audio output power:

1.5W or more (with 8 $\Omega$  load, 10% distortion)

#### Audio output impedance

4 ~ 16 $\Omega$  (Speaker and headphone)

### (FREQUENCY STABILITY)

#### Frequency accuracy: (RIT/XIT OFF)

More than  $\pm 10 \times 10^{-6}$

#### Frequency stability:

More than  $\pm 10 \times 10^{-6}$  (-10°C to 50°C)

#### (RIT/XIT OFF: at receive)

#### Reference oscillator frequency:

36MHz

**Note:** Circuit and ratings subject to change without notice due to developments in technology.

## CIRCUIT DESCRIPTION

### 1. Overview

- The TS-440 is a triple conversion type transceiver, incorporating a general coverage receiver, which uses 45.05 MHz as the first IF, 8.83 MHz as the second IF, and 455 kHz as the third IF.
- The TS-440 is compact, but allows for installation of an optional internal automatic antenna tuner operating in the amateur band from 3.5 MHz to 28 MHz and enables a wide range of antennas to be used.
- The TS-440 also contains a microprocessor-controlled digital PLL circuit which controls frequency in 10 Hz steps using a single crystal oscillator to implement high accuracy and stable frequency control.
- The TS-440 has the following major features:
  - (1) Selectable VFOs; VFO-A and VFO-B
  - (2) Direct frequency input using a numeric keypad
  - (3) 100-channel memory containing frequency band, and mode information (channel 90 to 99 for split fre-

- quency memory)
- (4) Memory scan in 10 channel groups and two types of program scan
- (5) RTTY (AFSK) mode available
- (6) Squelch circuit operational in all modes
- (7) Dual filters available to improve selectivity and S/N ratio (optional filter required)
- (8) IF shift, audio notch, IF filter switching, and RF ATT functions for convenient interference reduction
- (9) Large heat sink and cooling fan (100 W) enabling up to one-hour continuous transmit operation
- (10) Full and semi break-in circuits for CW
- (11) External-computer controllable (optional interface required)
- (12) Many easy-to-read meter functions such as the received signal strength (s-meter), transmitter power, SWR, and ALC level.

### 2. Frequency Elements

The TS-440 utilizes a triple conversion transmitter and receiver.

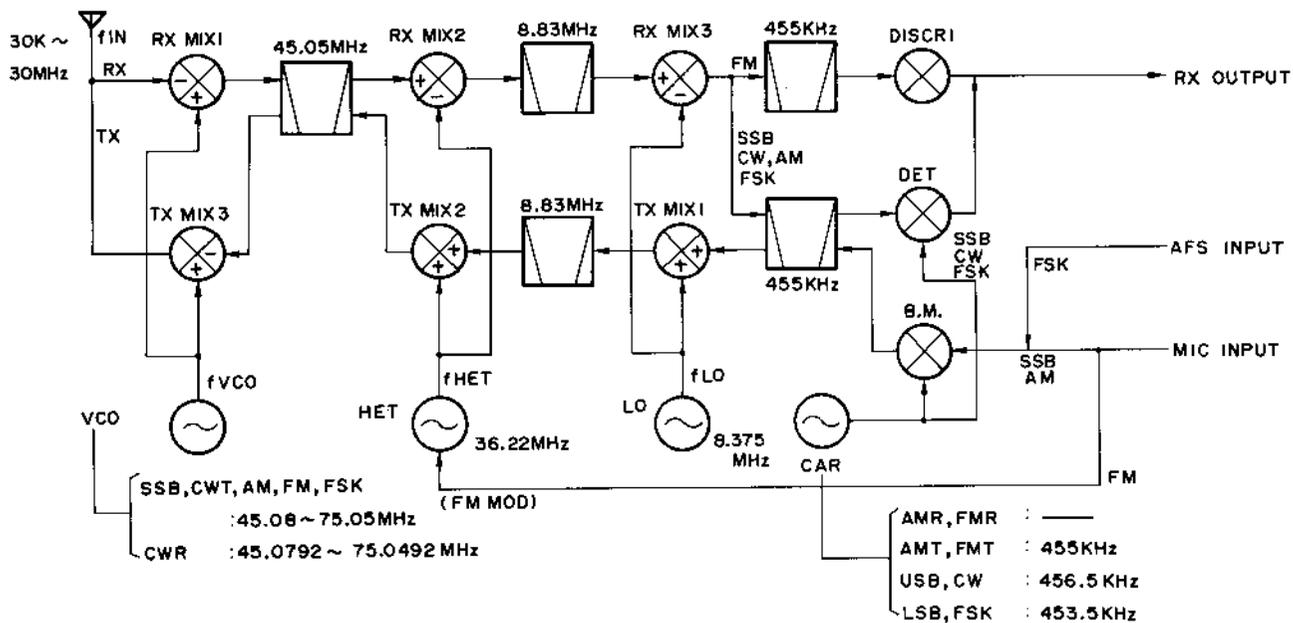


Fig. 1 Frequency configuration

The overall frequency configuration of the TS-440 is shown in Figure 1. The incoming received signal ( $f_{IN}$ ) is applied to the ANT terminal. This signal is mixed with the local oscillator signal ( $f_{VCO}$ ) in RX MIX 1 to obtain the first IF frequency. This signal is then mixed with the HET Oscillator signal ( $f_{HET}$ ) in RX MIX 2 to obtain the 2nd IF frequency. The signal is then mixed with the LO Oscillator signal ( $f_{LO}$ ) in RX MIX 3 to obtain the 3rd IF frequency. The signal is then combined with the CAR signal for detection.  $f_{IN}$  is expressed mathematically as follows:

tor frequency ( $f_{LO}$ ) to obtain the 3rd IF frequency. The signal is then combined with the CAR signal for detection.  $f_{IN}$  is expressed mathematically as follows:

$$f_{IN} = f_{VCO} - f_{HET} - f_{LO} - f_{CAR} \dots \dots \dots 1$$

CIRCUIT DESCRIPTION

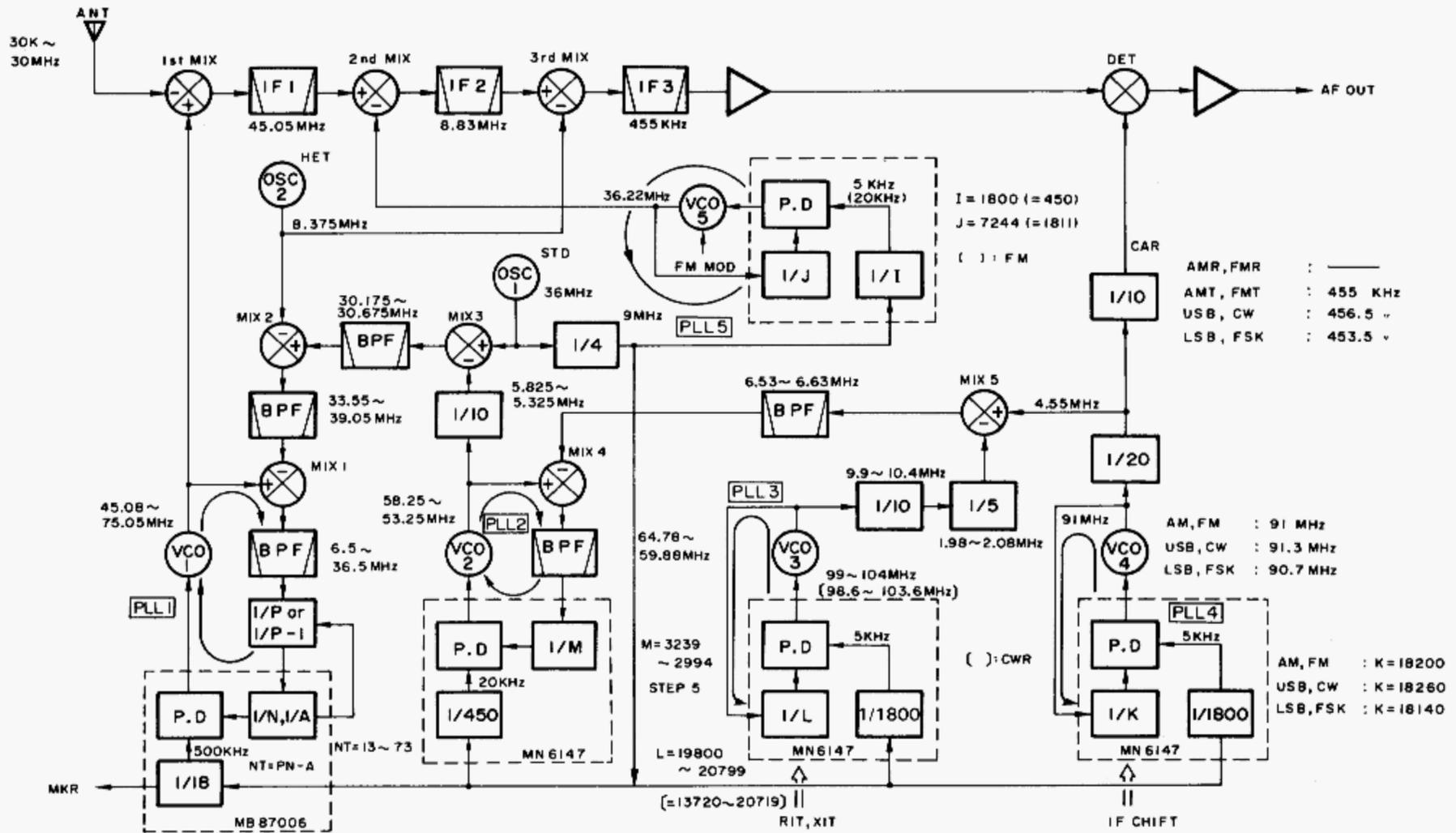


Fig. 2 PLL frequency configuration

As shown in figure 2, all received frequencies excluding the local oscillator frequency  $f_{LO}$  are generated in the PLL circuit. The frequencies generated in these loops are expressed as follows:

$$VCO5: \frac{f_{VCO5}}{J} = \frac{1}{4} \cdot f_{STD} \quad \therefore f_{VCO5} = \frac{J}{4I} f_{STD} \dots\dots 2$$

$$VCO4: \frac{f_{VCO4}}{K} = \frac{1}{4} \cdot f_{STD} \quad \therefore f_{VCO4} = \frac{K}{7200} f_{STD} \dots\dots 3$$

$$VCO3: \frac{f_{VCO3}}{L} = \frac{1}{4} \cdot f_{STD} \quad \therefore f_{VCO3} = \frac{L}{7200} f_{STD} \dots\dots 4$$

$$VCO2: \frac{f_{VCO2} + \frac{f_{VCO3}}{50} + \frac{f_{VCO4}}{20}}{M} = \frac{1}{4} \cdot f_{STD}$$

$$\therefore f_{VCO2} = \frac{M}{1800} \cdot f_{STD} - \frac{f_{VCO3}}{50} - \frac{f_{VCO4}}{20} \dots\dots 5$$

$$VCO1: \frac{f_{VCO1} - f_{LO} - f_{STD} + \frac{f_{VCO2}}{10}}{N} = \frac{1}{4} \cdot f_{STD}$$

$$\therefore f_{VCO1} = \frac{N}{72} f_{STD} + f_{LO} + f_{STD} - \frac{f_{VCO2}}{10} \dots\dots 6$$

Based on these formulas, the frequencies  $f_{VCO}$ ,  $f_{HET}$ , and  $f_{CAR}$  are expressed as follows:

$$+ \frac{K}{1440000} + 1) \cdot f_{STD} + f_{LO} \dots\dots 7$$

$$f_{HET} = f_{VCO5} = \frac{J}{4I} \cdot f_{STD} \dots\dots 8$$

$$f_{CAR} = \frac{f_{VCO4}}{200} = \frac{K}{1440000} f_{STD} \dots\dots 9$$

Formula 1 may now be rewritten as follows:

$$f_{IN} = \left( \frac{N}{72} - \frac{M}{180000} + \frac{L}{3600000} - \frac{J}{4I} + 1 \right) \cdot f_{STD} \dots\dots 10$$

Note that  $f_{LO}$  is not included in formula 10. That is, a received frequency is determined by the reference frequency  $f_{STD}$  and frequency division data I to N. Further analysis of formula 10 shows the following:

- i) Basically, frequency division data I to N contain no error because they are controlled by the microprocessor according to the operating frequency.
- ii) The accuracy of the operating frequency is equal to that of the reference frequency, because all frequencies other than  $f_{STD}$  in formula 10 are determined by the microprocessor.
- iii) The operating frequency does not change even if k or  $f_{LO}$  changes.

## CIRCUIT DESCRIPTION

$$I = 1800, J = 7244, K = 19800, L = 3239, M = 41$$

$$\therefore f_{IN} = 0.388 f_{STD} \dots\dots\dots 11$$

When  $f_{IN} = 30$  MHz (USB mode) in formula 10,  $f_{IN}$  and  $f_{STD}$  have the following relationship:

$$I = 1800, J = 7244, K = 19800, L = 3239, M = 73$$

$$\therefore f_{IN} = 0.833 f_{STD} \dots\dots\dots 12$$

Since the precision of the reference crystal oscillator used in the TS-440 is 10 ppm (-10 to 50°C) and the receiver system has the characteristics shown in items i) and ii), the total accuracy is stable at any point from 30 kHz to 30 MHz. The maximum amount of frequency shift is only  $\pm 300$  Hz (see formula 12). The characteristic shown in item iii) enables variable band functions such as IF shift to be implemented, using the microprocessor. The microprocessor also is used to set carrier points by adjusting  $f_{CAR}$ , and to set and adjust the amount of IF shift.

So far received frequencies in the SSB mode have been dis-

cussed. For receive modes other than SSB, and in transmit mode, operating frequency is determined by the reference frequency and frequency division data.

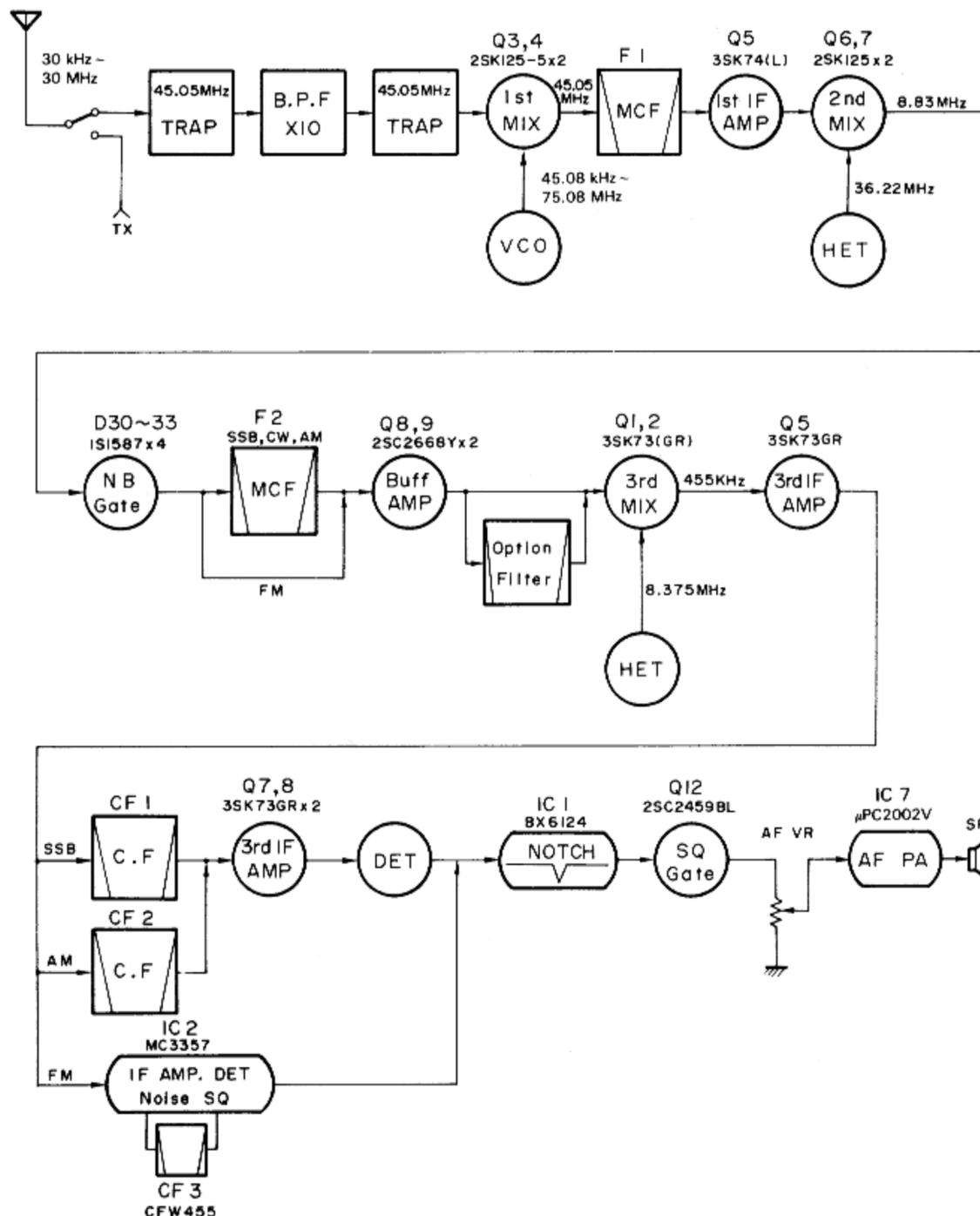
In CW receive mode,  $f_{VCO}$  is shifted down 800 Hz and used as  $f_{VCO3}$ . In AM or FM receive mode,  $f_{CAR}$  generation is stopped. In FM receive mode,  $f_{HET}$  is modulated by adding audio signals to VCO5 from the microphone. FSK (RTTY) is transmitted in LSB mode and uses AFSK by adding audio signals externally.

The type of frequency displayed differs, depending on the mode, as shown in Table 1.

Mode	Displayed frequency
USB, LSB, FSK	Carrier point frequency
CW	Transmission carrier frequency
AM, FM	IF filter center frequency

Table 1 Displayed frequencies

### 3. Receiver Circuit Description



## CIRCUIT DESCRIPTION

Signals from the ANT pin are fed into the RAT pin of the RF unit via the transmit/receive switching relay. The signals then go to the 10 BPFs through the approx. 20 dB attenuator circuit, the first stage of the first IF trap circuit, and the low pass filters (which pass only 500 kHz or less). The signal then goes through the second stage of the first IF trap circuit, and is mixed with the VCO signal and converted into the first IF signal of 45.05 MHz in the first mixer, consisting of Q3 and Q4 (2SK125-5). The VCO circuit consists of Q21 to Q24 (2SC2668Y) and oscillates in four bands from 45.05 MHz to 75.05 MHz. Oscillator frequencies are controlled by DC signals from the PLL unit.

The first IF signal of 45.05 MHz is passed through the MCF (F1), which is used in both receive and transmit, and is amplified by the first IF amplifier Q5 (3SK74L). In the second mixer, consisting of Q6 and Q7 (2SK125), the first IF signal is mixed with the heterodyne oscillator signal (36.22 MHz) from the PLL circuit, amplified by Q12 (2SC2668Y) to obtain the second IF signal (8.83 MHz). The second IF signal of 8.83 MHz goes through the gate of the noise blanker. In modes other than FM, the signal then goes through the MCF (F2) and is fed into the IF unit through buffer amplifiers Q8 and Q9 (2SC2668Y).

When the optional 8.83 MHz filter is connected, the second IF signal is then fed from the IF unit into the optional filter. In the third mixer, consisting of Q1 and Q2 (3SK73GR), the second IF signal is mixed with 8.375 MHz signal generated by IF unit's heterodyne oscillator circuit, consisting of Q53 and Q54 (2SC2458Y), and converted into the third IF signal (455 kHz). The third IF signal is then amplified by Q5 (3SK73GR). A diode switch is used to route the signal to either the FM or SSB circuits.

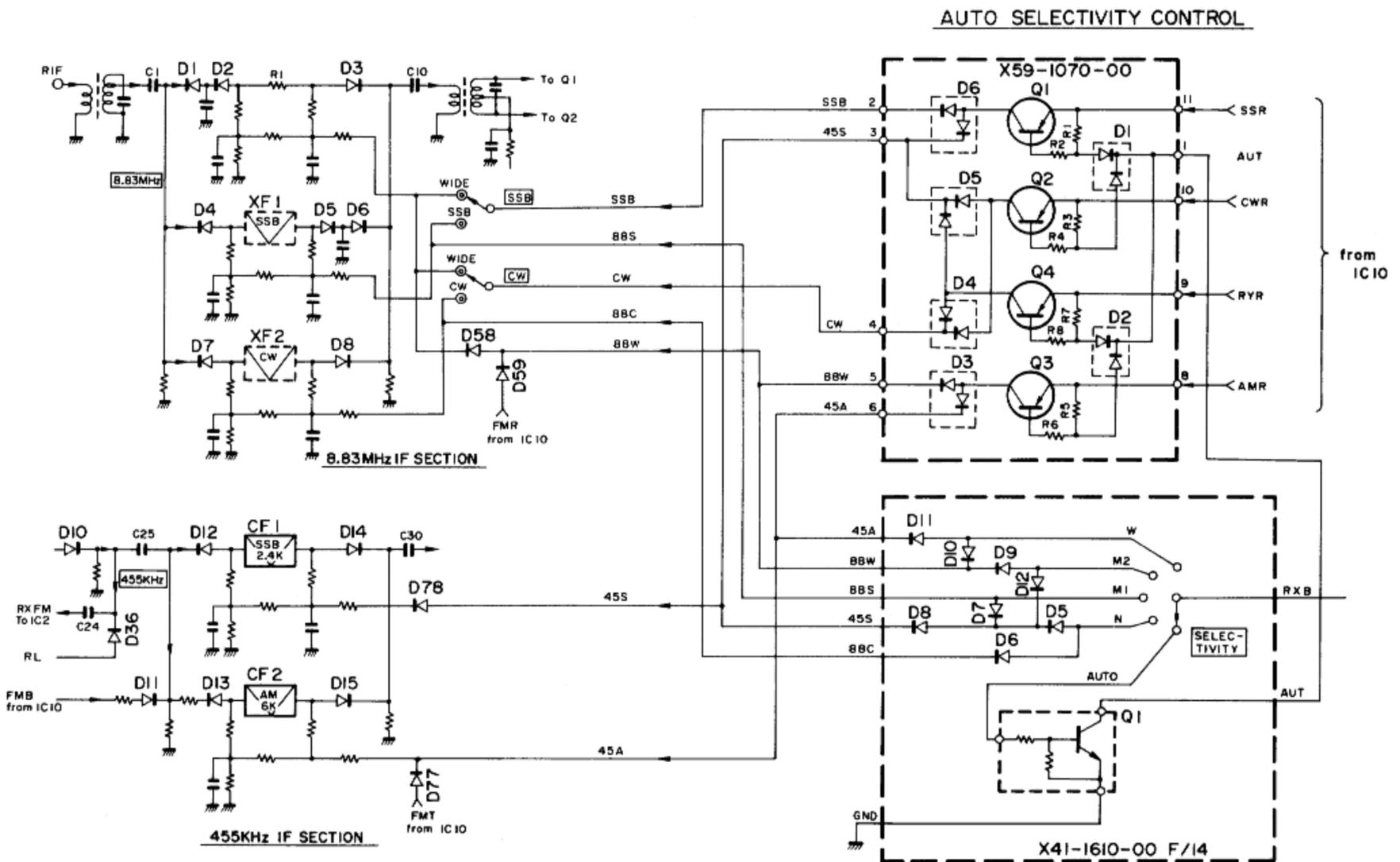
In SSB mode, the third IF signal goes through the SSB ceramic filter (XF3). In AM mode, the third IF signal goes through the AM ceramic filter (XF4). In either mode, the third IF signal is then amplified by Q7 and Q8 (3SK73GR) and detected. In FM mode, the third IF signal goes through the FM ceramic filter (XF5). The signal is then sent to the FM IF, IC2 (MC 3357) for amplification and detection. IC2 also contains an FM noise squelch circuit.

The detected SSB/AM signal is passed through the notch circuit, consisting of hybrid IC IC1 (BX6124) and squelch gate Q12 (2SC2459BL). The signal then goes through the AF volume control and is amplified to the appropriate level by AF amplifier IC7 (UPC2002V).

### 1) Selectivity circuit

Figure 4 is a selectivity circuit diagram. In auto mode, the appropriate bandwidth filter is automatically selected according to mode. When an optional filter is used, two filters are available. Tables 2 and 3 shows the various combinations

of bandwidth available when optional filters are used. In FM mode, the selectivity switch does not operate and a single dedicated FM filter is used. Optional filters operate only in receive and are separate from the filters used in transmit.



## CIRCUIT DESCRIPTION

### Filter selective

#### AUTO MODE

MODE	WITHOUT OPTION		OPTION INSTALLED	
	8.83MHz	455kHz	8.83MHz	455kHz
SSB	Through	CF1	XF1	CF1
CW	Through	CF1	XF2	CF1
AM	Through	CF2	Through	CF2
FSK	Through	CF1	XF2	CF1
FM	Through	—	Through	—

XF1: YK-88S or YK-88SN  
XF2: YK-88C or YK-88CN

Table 2

Item	Rating
Center frequency $f_0$	45.05 MHz
Center frequency deviation	$f_0 \pm 1$ kHz at 3 dB
Pass bandwidth	$\pm 9.6$ kHz or more at 3 dB
Attenuation bandwidth	$\pm 28$ kHz or less at 10 dB
Ripple	0.7 dB or less
Insertion loss	2.0 dB or less
Guaranteed attenuation	30 dB or more with $\pm 1$ MHz (Except spurious)
Final impedance	$2 \text{ k}\Omega \pm 10\%$ /L characteristic

Table 4 MCF (L71-0259-05) (RF UNIT F1)

Item	Rating
Center frequency $f_0$	$8830 \text{ kHz} \pm 0.5 \text{ kHz}$
Pass bandwidth	$\pm 3$ kHz or more at 3 dB
Attenuation bandwidth	$\pm 12$ kHz or less at 18 dB
Guaranteed attenuation	30 dB or more within $f_0 \pm 1$ MHz
Ripple	0.5 dB or less
Insertion loss	1.0 dB or less
Final impedance	$2.5 \text{ k}\Omega / 3 \text{ pF}$

Table 6 MCF (L72-0260-05) (RF unit F2)

Item	Rating
Center frequency $f_0$	$455 \text{ kHz} \pm 0.2 \text{ kHz}$ at 6 dB
6 dB bandwidth (total)	$\pm 1.1 \sim 1.3$ kHz
60 dB bandwidth	4.5 kHz or less
Guaranteed attenuation	60 dB or more (at 0.1 ~ 1 MHz)
Spurious (600 ~ 700 kHz)	40 dB or more
Ripple with bandwidth	2 dB or less at 60 dB
Insertion loss	2 dB or less
Temperature	$-10^\circ\text{C} \sim +50^\circ\text{C}$
Input and output impedance	$2 \text{ k}\Omega$

#### MANUAL MODE

SELECT	WITHOUT OPTION		OPTION INSTALLED	
	8.83MHz	455kHz	8.83MHz	455kHz
N	NO RX		XF2	CF1
M1			XF1	CF1
M2	Through	CF1	Through	CF1
W	Through	CF2	Through	CF2

XF1: YK-88S or YK-88SN  
XF2: YK-88C or YK-88CN

Table 3

Item	Rating
Center frequency $f_0$	455 kHz
6 dB bandwidth	$\pm 2$ kHz or more
40 dB bandwidth	7.5 kHz or less
Insertion loss	6 dB or less
Guaranteed attenuation (within 455kHz $\pm 100$ kHz)	35 dB or more
Input and output impedance	$2.0 \text{ k}\Omega$

Table 5 Ceramic filter (L72-0355-05) (IF UNIT CF2)

Item	Rating
Center frequency $f_0$	$455 \text{ kHz} \pm 1 \text{ kHz}$
6 dB bandwidth	$\pm 6$ kHz or more
50 dB bandwidth	$\pm 12.5$ kHz or less
Ripple (within 455 kHz $\pm 4$ kHz)	3 dB or less
Insertion loss	6 dB or less
Guaranteed attenuation (within 455 kHz $\pm 100$ kHz)	35 dB or more
Input and output impedance	$2.0 \text{ k}\Omega$

Table 7 Ceramic filter (L72-0315-05) (IF unit CF3)

Item	Rating
Center frequency $f_0$	8.830 MHz
Attenuation bandwidth	$\pm 50$ kHz or more at 3 dB
Guaranteed attenuation	35 dB or more at 9.285 MHz 45 dB or more at 9.74 MHz
Insertion loss	6 dB or less
Ripple	1.0 dB or less
Input and output impedance	$330 \Omega$
Max. voltage (DC)	50 V (Min.)

## CIRCUIT DESCRIPTION

### 2) AF notch circuit

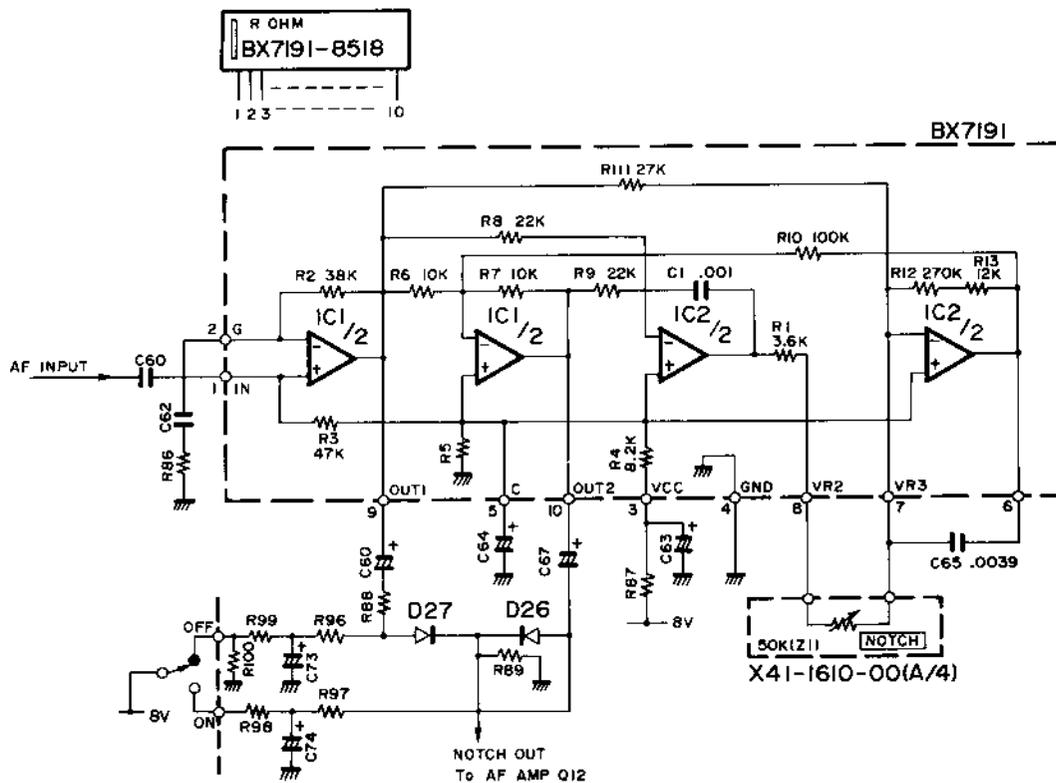


Fig. 5 NOTCH circuit

The hybrid IC1 in the IF unit is an audio notch circuit. Figure 5 shows its equivalent circuit. This circuit forms state-variable bandpass filter, also known as a bi-quad filter. The notch frequency can be changed using the notch control variable resistor. Since the circuit consists of the hybrid IC, stable attenuation characteristics can be obtained electrically and thermally. The range of variable notch frequencies is 400 Hz to 2600 Hz.

The notch frequency is determined by the following two formulas.

- 1)  $f_N \cong \sqrt{R6/2\pi \cdot (R1 + \text{Notch VR}) \cdot R8 \cdot R10 \cdot C1 \cdot C65}$ ..... 1
- 2)  $R6 \cdot (R12 + R13) \cong R10 \cdot R11$ ..... 2

If a variable resistor is used for resistor NOTCH VR, the notch frequency can be controlled according to formula 1). The notch frequency range is from 400 to 2600 Hz, and attenuation is from 25 to 50 dB.

## CIRCUIT DESCRIPTION

### 3. Transmitter Circuit Description

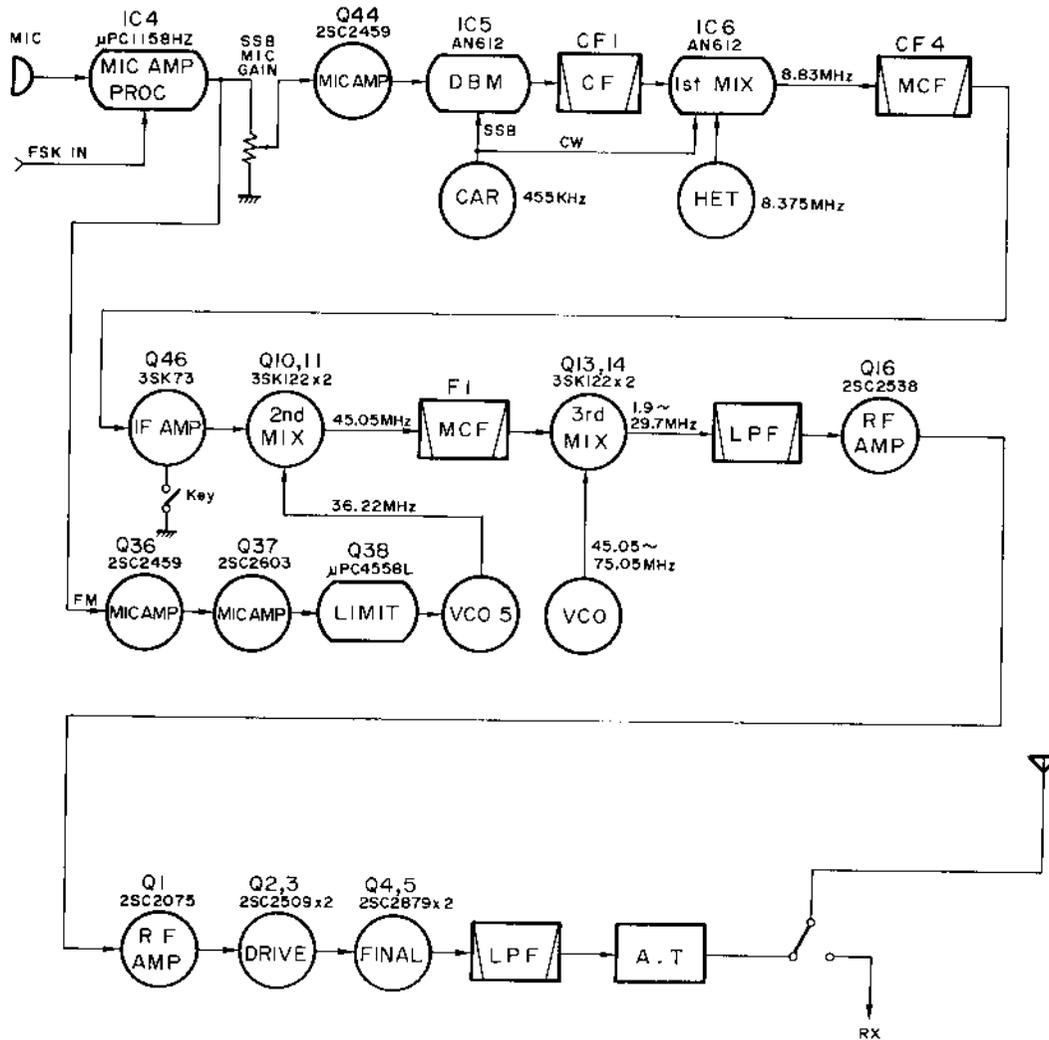


Fig. 6 Transmitter circuit configuration

In SSB, CW, AM, or FSK mode, the transmitter system uses triple conversion. In FM mode, the transmitter system uses double conversion using PLL modulation.

Audio signals from the microphone are applied to the MIC pin (connector (21)) of the IF unit and are separated into SSB modulation and VOX signals. The SSB signal is amplified approx. 8 dB by IC4 (μPC1158HZ). AFSK audio signals from the AFSK IN pin (back panel) are also applied to IC4.

IC4 functions as a SPEECH processor. Output from IC4 is distributed to the MIC GAIN control (front panel) and FM circuit (RF unit). In SSB mode, the signal applied to the MIC GAIN control is sent back to the IF unit (connector (23) MV2), amplified by Q44 (2SC2459), and supplied to the balanced modulator IC5 (AN612). In FM or CW mode, Q44 does not operate because a cut-off voltage is supplied to its emitter via diodes D82 and D46. The signal converted to 455 kHz

## CIRCUIT DESCRIPTION

DSB by IC4 goes through the SSB transmit switching diodes D17 and D18, filter switching diodes D14 and D12, and SSB ceramic filter CF1, to obtain the SSB signal. The SSB signal then goes through the transmit switching diode D36 and is fed into the transmit first mixer, IC6, where the SSB signal is mixed with the output from the 8.375 MHz oscillator in the IF unit, and converted to 8.83 MHz. In CW or FM mode, the carrier signal from the PLL unit does not go through IC5 BM or the 455 kHz filter. These carrier signals are applied to IC6 via switching diodes D53 and D54. The output signal from IC6 goes through the MCF to remove spurious components, and is amplified by the IF amplifier Q46 (3SK73) and sent to the RF unit. Q46 provides ALC control and CW keying.

In the transmitter second mixer, consisting of Q11 and Q12, (3SK122), the 8.83 MHz transmit IF signal input to the RF unit is mixed with HET oscillator signal (36.22 MHz) from the PLL unit and converted to 45.05 MHz signals. The 45.05 MHz signal goes through D23 and the MCF to remove any spurious components. The 45.05 MHz signal then goes through D27 and is supplied to the transmit third mixer consisting of Q13 and Q14 (3SK122). In the third mixer the signal is mixed with VCO signal (Q21 to Q24) amplified by Q12 (2SC2668) and converted to the required transmit frequency (1.8 to 29.7 MHz). The signal from the third mixer goes through the low pass filters C156, C158, C159, and L89, and is amplified by the wide band amplifier Q15 (2SC2570). The signal then goes through the wide band transformer T19 and low pass filters C164, C165, and L90, and is further amplified by wide band amplifier Q16 (2SC2538). The signal from the Q16 goes through the output transformer T20 and is used as the drive output.

In FM mode, the PLL VCO is directly modulated. The audio signal from IF unit IC4 (UPC1158HZ) is fed into the RF unit via the FMI pin. In the RF unit, the audio signal is amplified by Q36 (2SC2459) and Q37 (2SC2603), and goes through the limiter circuit consisting of Q38 (UPC4558C) and low pass filter circuit, and is sent to the PLL unit via the FMD pin. In the PLL unit, the 36.22 MHz VCO is modulated. Q39 (2SC2603) is a switching circuit to prevent the modulated signals from being emitted from the PLL unit in a mode other than FM.

For "S" model radios the output from the RF unit is amplified to a 100 W power level by Q1 (2SC2075), Q2 and Q3 (2SC2509), and Q4 and Q5 (2SC2879) in the final unit. The 100 W output goes through the LPFs which differ by bands, and is sent as output to the antenna via the AT unit and transmit/receive switching relay. SWR and ALC detection is performed at the output of the LPFs.

### 1) Antenna tuner

The antenna tuner operates when the AUTO/THRU switch is in the AUTO position and the AT TUNE switch is ON. The antenna tuner is driven in the CW mode and power is reduced to 50 W by the microcomputer regardless of the mode selected before the AT TUNE switch was turned ON. The range of operating frequencies is determined by a microcomputer program, and is from 3.5 MHz to 30 MHz.

#### • AT unit operation

Power transmitted by the final unit passes through the current and voltage detecting transformers L1 and L2 using toroidal cores. Current and voltage components detected by the transformers are supplied to pins 9 and 13 of IC2 for wave shaping and their phases are compared by IC3 HD10131. The output from pin 3 of IC3 depends upon the phase of the voltage and current waveforms applied to IC3. The signal from IC3 pin 3 is sent to pins 10 and 15 of buffer IC IC3 HD10125. Output from pins 12 and 13 of IC3 goes through level shift Zener diodes D5 and D6 to control the input circuit of motor drive IC IC5 BA6109U2. The output signal is used to drive motor M1 to adjust the variable capacitor VC1 so that the phase difference between voltage and current components is reduced.

The current and voltage components output from the current and voltage detecting transformers is also supplied to the voltage comparator IC1 NJM2903D. The comparator output is used by motor drive IC IC6 BA6109U2 to drive motor M2 to adjust variable capacitor VC2 so that the amplitude difference is reduced. That is, the phase control variable capacitor VC1 is controlled so that the current is in phase with the voltage and the voltage control variable capacitor VC2 is controlled so that the amount of amplitude difference between the current and voltage is reduced (SWR1, an SWR of 1 to 1, is obtained when the current and voltage are in phase and the amount of amplitude difference is 0). VC1 and VC2 are designed to operate independently of each other, but since phase difference affects the amount of amplitude difference and vice versa, VC1 and VC2 will normally rotate together.

Forward and reflected waves detected by the filter unit are converted to SWR control signals in the SWR arithmetic circuit in the control unit and are sent to the ISW pin of the AT unit. Since the SWR control signals are current waveforms, the signals are converted from I to V waveforms by IC8 (b/4) in the AT unit and to obtain the corresponding voltage mode SWR signals are generated. The SWR signals are then fed into the SWR comparator IC8 (C/4). The reference voltage pin 9 of the IC8 (C/4) is supplied with a voltage corresponding to an SWR of 1.25 to 1 via a potentiometer. Therefore, when the actual SWR value exceeds 1.25, pin 8 of SWR comparator IC8 (C/4) is H, so the motor drive voltage control transistor Q5 turns on and the collector of Q4 is supplied with voltage from pin 14S. The voltage is also used to turn the tuning LED on. The inverted input pin of IC8 (d/4) is supplied with triangular waves generated by IC7, and its non-inverted input pin is supplied with the above SWR vol-

## CIRCUIT DESCRIPTION

waves changing from continuous waves to relatively low duty pulses. Q1 is driven by this voltage waveform to control Q2, which is connected to the collector of Q4 in series and motor drive voltage is generated.

If the motor turns too fast, the SWR value will be smaller than the motor stop value because of the inertia of the motor. As a result, the motor will continue to operate even if

the motor stop signal is sent and the SWR value will continue to be greater than the motor stop value, causing the motor stop signal to turn off. That is, the motor will not stop and it will be difficult to obtain a match. If the motor speed is too slow, it will take a long time to satisfy a matching condition. The TS-440 therefore controls the motor speed according to changes in SWR.

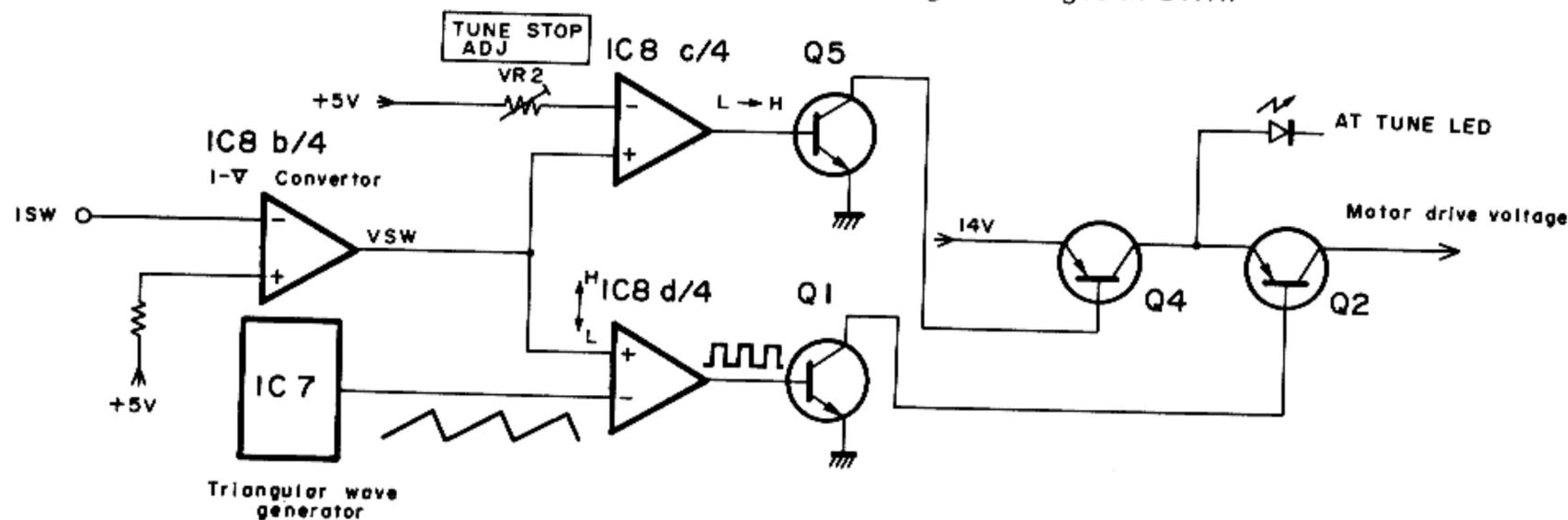


Fig. 7 Antenna tuner circuit

The antenna coupler is a T type. Six relays RL100 to RL105 are used to change taps within the range 3.5 MHz to 30 MHz.

### 2) Cooling fan circuit

The final unit contains the temperature-sensitive thermistor TH1 thermally coupled with final transistor Q4. When temperature on the surface of Q4 reaches approx. 50°C, the fan start comparator Q9B operates (H level), causing Q8 to turn on to operate the fan. During operation of the fan, temperature protection comparator Q9A is at a L level, so the temperature protection circuit does not operate.

When temperature on the surface of Q4 goes down to 45°C, the cooling fan turns off.

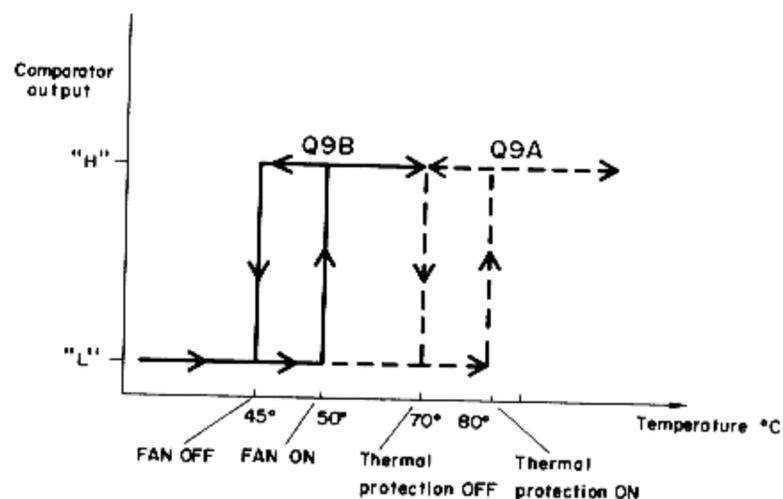


Fig. 8 temperature protection operation

- **Final temperature protection circuit**

When the temperature of the final transistor Q4 rises up to approx. 80°C, the temperature protection comparator Q9A turns on (H level), Q1 in the filter unit also turns on, and a minus DC voltage is supplied to the ALC line, reducing the transmitter output to zero. (The TS-440 does not return to a receive state.) When the temperature of the final transistor Q4 falls to approx. 70°C, the protection circuits turns off allowing the transmitter to operate again.

- **SWR protection circuit**

When antenna VSWR is bad, or the reflected wave is too large, because the auto antenna is tuning for example, L42 and L43 detect the state and its output is rectified. The rectified signal is then amplified by Q2 to control the ALC voltage so that drive power is reduced. As a result, load on the final unit is reduced.

- **SWR automatic arithmetic circuit**

The TS-440 uses the automatic arithmetic circuit in the AT-250. The forward wave voltage  $V_{SF}$  and reflected wave voltage  $V_{SR}$  from the filter unit are fed into the analog arithmetic circuit of the switch unit, and used to set the voltage level of IC8 pin 2 ( $5V + V_{SR}/V_{SF}$ ). Output voltage from the pin 2 is shifted by IC5 to move the needle in the SWR meter.

IC5 contains a level shift/meter amplifier and an auto tuner V-I converter. IC7 contains a square wave generator and a voltage comparator. IC8 contains an integration circuit.

### CIRCUIT DESCRIPTION

$V_{SF}$  is compared with voltage from IC8 pin 6 (5.5 V). When SWR increases,  $V_{SF}$  lowers and the voltage level of IC8 pin 8 rises. At IC7 pin 3, a triangular wave is monitored. The triangular wave is compared with the wave from IC8 pin 8 and output. The triangular wave is converted to a square wave by IC10 and sent to switch Q3 and Q4. This voltage is used as the SWR control voltage.

Output voltage from IC8 pin 2 consists of the voltage compared with  $V_{SR}/V_{SF}$  and +5 DC voltage. It is distributed to IC4 the level shift/meter amplifier to move the needle in the SWR meter and IC5 the V-I convertor to control the AT440.

VR14 is used to adjust the SWR meter ZERO point. VR13 is for SWR meter adjustment

### 3) FULL/SEMI BREAK-IN and VOX circuits

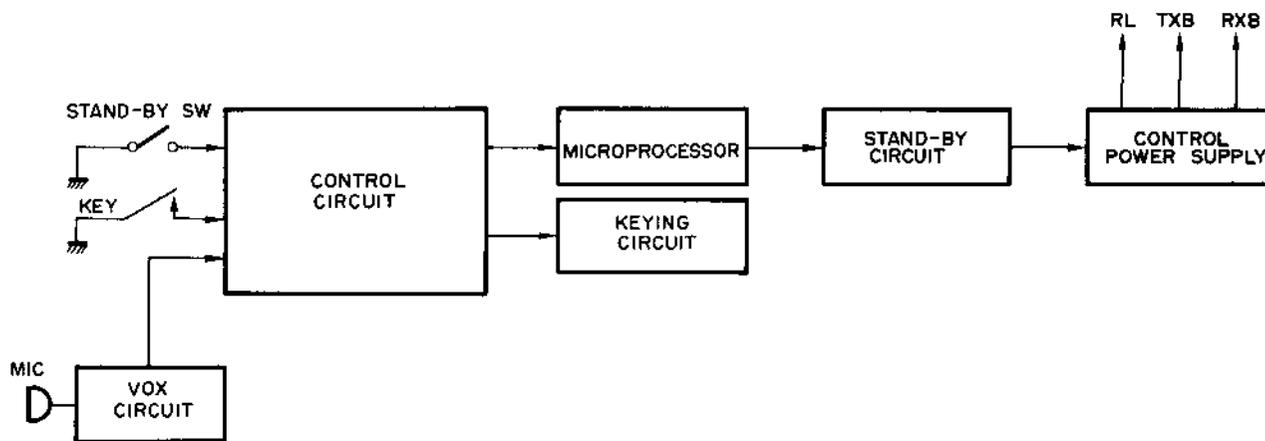
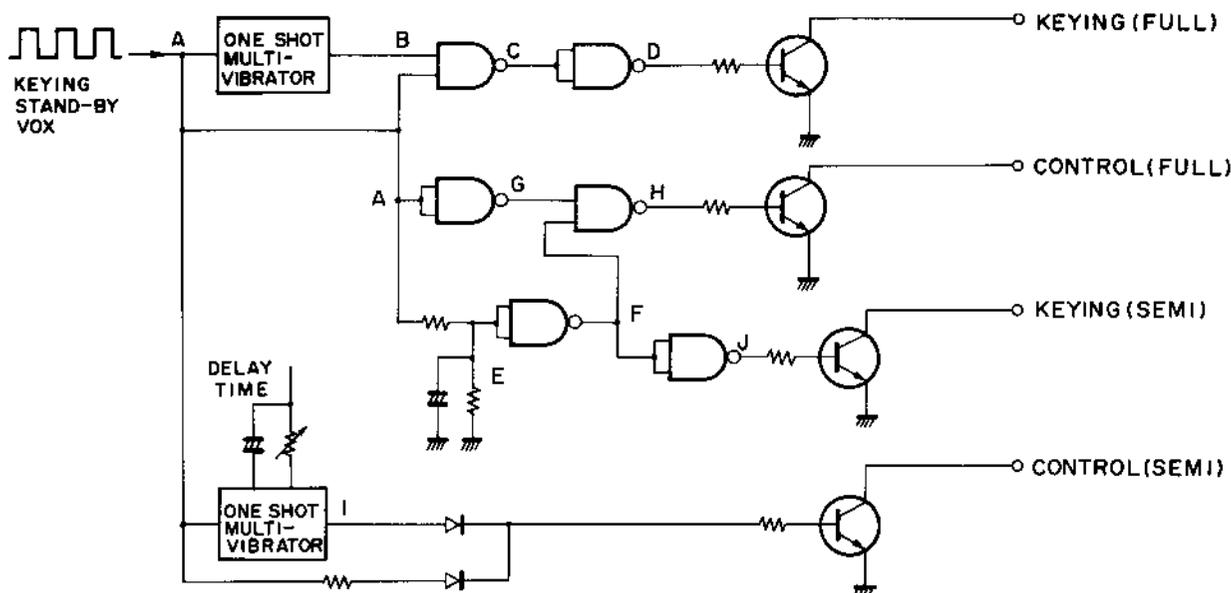


Fig. 9-1 FULL/SEMI BREAK-IN block diagram

When the standby switch, the key, or the VOX switching transistor are activated, a ground is applied to the input pin of the control circuit, which causes a standby signal to be fed to the microprocessor to determine if a valid transmit condition has been met. When that condition has been met, the

standby circuit in the IF unit will be turned on. A keying signal is generated by the control circuit, whenever the key is depressed, to control the keying circuits in the IF unit. This keying signal is also used as the transmit/receive signal during break-in operations.



## CIRCUIT DESCRIPTION

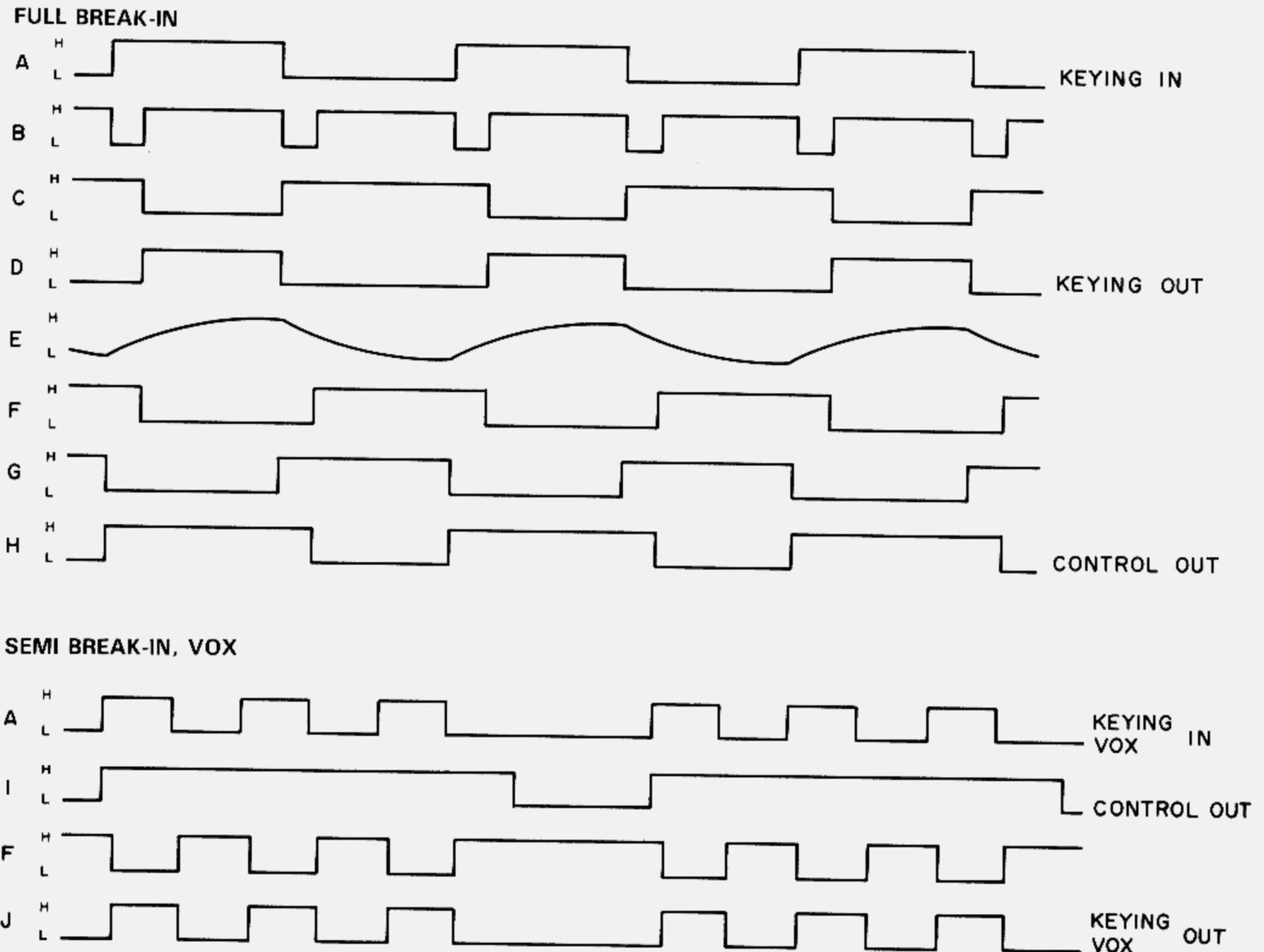


Fig. 9-3 FULL/SEMI BREAK-IN timing chart

The above timing charts show the timing for standby and keying signals.

When an input from the CW key is supplied to point A as shown in the above figure during full break-in operation, the one-shot multi-vibrator and gate circuits generate control (full) and delayed keying (full) signals. After the fundamental timing signal, RL (12V) for reception and transmission rises, the keying wave also rises, and when the key is off, RL falls according to the preset time constant.

Semi-break-in operation is synchronized to VOX. When a signal is supplied to point A, the VOX delay time multi-vibrator determines the VOX time constant. The input signal is converted to a keying (semi) signal by the gate circuit.

These keying semi/full and control semi/full signals are converted to appropriate break-in VOX mode signals us-

ing the slide switch. The control signal is checked by the microcomputer to see whether transmission is to be performed. The control signal is then used to switch CRL in the IF assembly unit and generate RL (12 V). TXB (transmit B+) (8.8 V) is generated, synchronized to RL. The receive control signal RXB (receive B+) (8.8 V) turns on/off, synchronized to the inverted TXB signal, that is, RL.

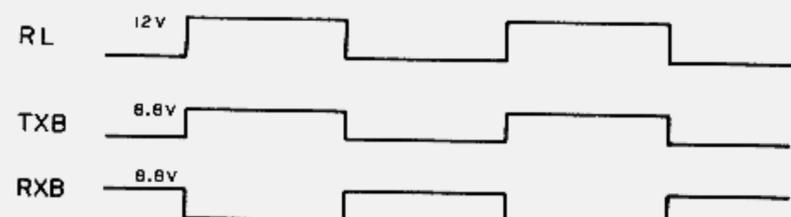


Fig. 10 STANDBY keying timing chart

## CIRCUIT DESCRIPTION

### 4) Speech processor

IC4 in the IF unit functions as the first stage microphone amplifier or audio speech processor. When the processor switch is off, IC4 functions as a 20 dB microphone amplifier. When the processor switch is on, IC4 functions as an up to 40 dB

gain amplifier with ALC. When the processor switch is on, 8 VDC is supplied to the base of the gain adjustment switching transistor, Q41, driving the feedback amplifier.

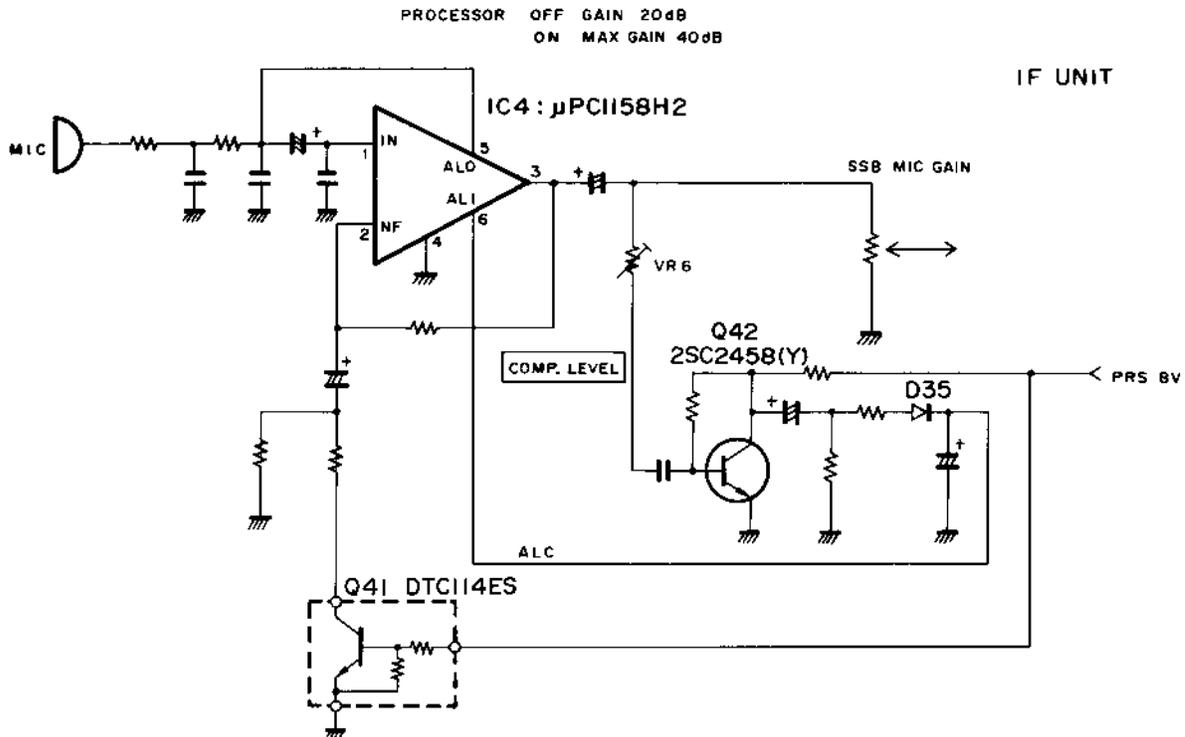


Fig. 11

## 4. PLL Circuits

### Theory of PLL circuit operations

The TS-440 PLL circuit uses a reference frequency of 36 MHz and consists of five PLL loops covering the range of frequencies from 30 kHz to 30 MHz in 10 Hz steps. The PLL circuit has an IF shift function which is implemented by inserting carrier frequencies between PLL loops. The PLL loops include a carrier circuit PLL loop and an HET circuit PLL loop which generates a constant frequency of 36.22 MHz. Frequency division for these PLL loops is controlled by the microprocessor. In all PLL loops phase comparison is made using the reference frequency  $f_{STD}$  (frequency control using a single crystal oscillator).

Figure 12 is the PLL circuit block diagram.

The reference frequency ( $f_{STD}$ ) is generated by a 36 MHz crystal oscillator and Q21 (2SC2787). Reference frequency signals are fed into the main loop's IC11 (SN16913P) via a buffer consisting of Q22 and Q23 (2SC2668). The signal is also fed into IC13 (SN74S112) via a buffer consisting of Q24 (2SC2668). In IC13, the signals are frequency divided to generate a 9 MHz signal. The 9 MHz signal is used as the

- PLL5

PLL5 consists of IC18 (MN6147) and its associated loop components. VC05, Q36 (2SK192A), is locked at a frequency of 36.22 MHz. The 9 MHz reference frequency signal is supplied to pin 3 of IC18, where the signal is divided by 1800 (450 in FM mode) to generate a 5 kHz (20 kHz in FM mode) signal used for comparison. VC05's output signal is supplied to IC18 pin 16 via Q37 (2SC2668), where the signals are frequency divided by 7244 (1811 in FM mode). The phase of the signal is then compared with that of the 5 kHz (20 kHz in FM mode) signal by the phase comparator and the VC05 oscillation frequency is locked. Frequency division data is supplied by digital unit (DA0 to DA3 and CK4).

As described above, the dividing ratio used varies depending on which mode the TS-440 is in, FM mode or SSB. This is because the apparent time constant is increased without changing the active LPF constant so that the PLL signals can be modulated easily and reducing distortion during FM transmission. In modes other than FM, the amount of frequency shift due to mechanical vibrations is reduced because the apparent time constant is reduced.

## CIRCUIT DESCRIPTION

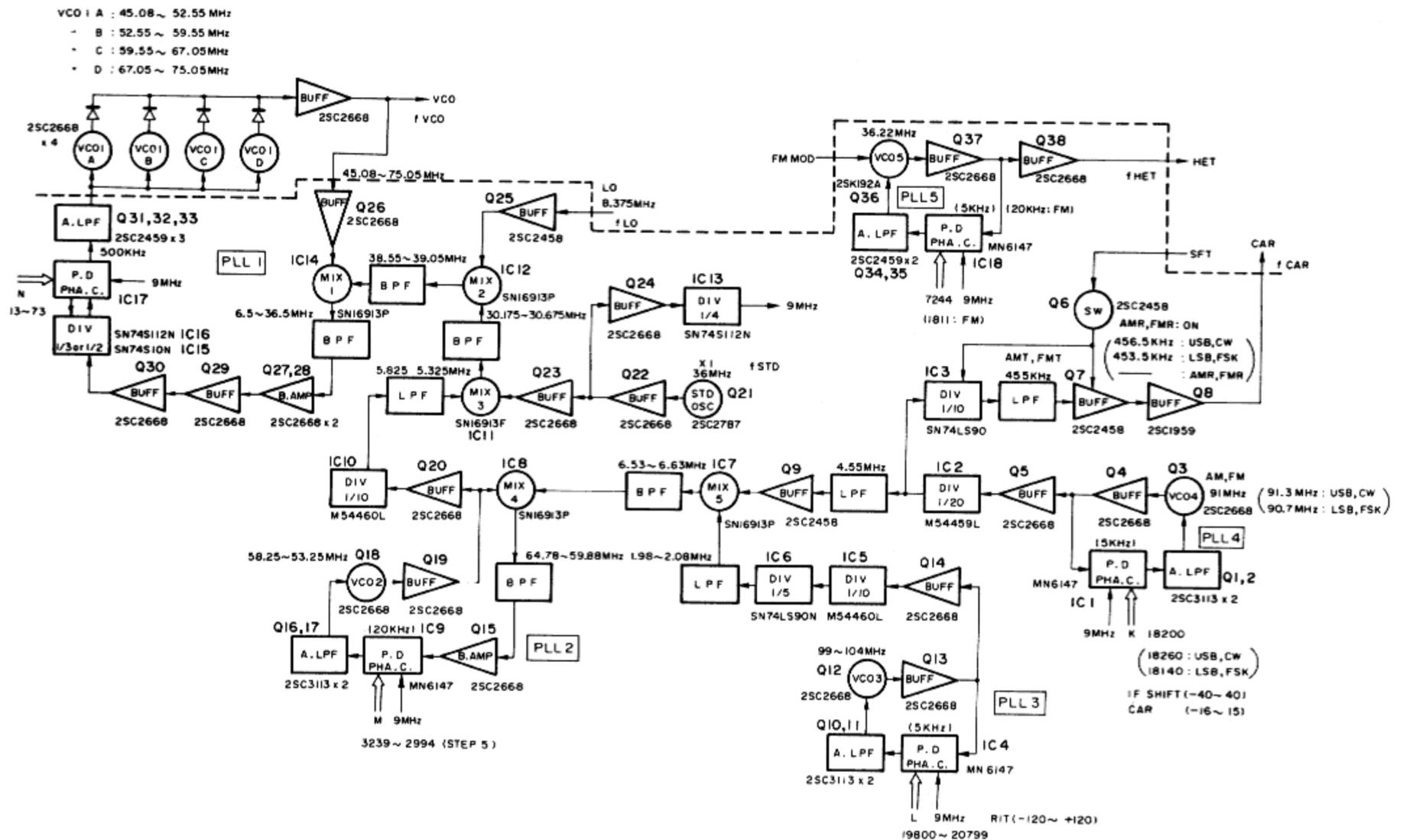


Fig. 12 PLL circuit block diagram

### • PLL4

PLL4 consists of IC1 (MN6147) and its associated loop circuit. VCO4, Q3 (2SC2668), is locked at a frequency of approximately 91 MHz, which differs depending on the operational mode. The 9 MHz reference frequency is applied to pin 3 of IC1, where the signal is divided by 1800 to generate the 5 kHz signal for frequency comparison. The output of VCO4 is supplied to IC1 pin 16 via buffer amplifier Q4 (2SC2668). In IC1, the output is divided by an appropriate division ratio (18200 or so) which differs depending on the mode. The phase of the signal is compared with that of the 5 kHz reference signal by the phase comparator and the VCO4 oscillation frequency is locked. Frequency division data is sent from the digital unit (DA0 to DA3 and CK3).

The output from PLL4 goes through buffer amplifier Q5 (2SC2668) and is divided by 20 in IC2 (M54459L). The signal is further divided by ten in the carrier circuit of IC3 (SN74LS90N) and then fed into the IF unit as the carrier signal via the L.P.F., and buffer Q7 (2SC2458) and Q8 (2SC1959). In AM or FM receive mode, switching circuit Q6 (2SC2458) operates when an SFT signal is sent, and as a result, IC3, Q7, and Q8 are stopped to cut carrier signals.

The PLL4 output signal also goes through the L.P.F. and buffer amplifier Q9 (2SC2458) and is fed into the mixer in the main loop, where the signal is used to form the digital VFO signal. As a result, the operating frequency does not change even if the carrier frequency is changed, which

ensures a constant carrier frequency. In SSB, CW, or FSK reception mode, the carrier may be shifted  $\pm 1$  kHz or more and the carrier point can be adjusted in the range from  $-400$  Hz to  $+350$  Hz.

### • PLL3

PLL3 consists of IC4 (MN6147) and its associated loop components. VCO3, Q12 (2SC2668), is locked in the range of 99 MHz to 103.995 MHz. The 9 MHz reference frequency signal is supplied to pin 3 of IC4, where the signal is divided by 1800 to generate the 5 kHz signal for frequency comparison. The output of VCO3 goes through buffer amplifier Q13 (2SC2668) and is applied to IC4 pin 16. In IC4, the output is divided by L and the phase of the signal is compared with that of the 5 kHz reference signal by the frequency comparator, and VCO3 oscillation frequency is locked (in 5 kHz steps). The division ratio, L, is supplied by the microprocessor, in the digital unit, (DA0 to DA3 and CK2). L is in 1000 steps (19800 to 20799) corresponding to 0.00 kHz to 9.99 kHz. In CW receive, in order to obtain 800 Hz beat signals in the operation frequency display, the L is shifted  $-80$  (19720 to 20719) and when RIT/XIT operates, the L is changed so that  $f_{VCO}$  is shifted  $\pm 1.2$  kHz or more. In AM or FM mode, the L is shifted by 10 steps to change  $f_{VCO}$  by 100 Hz steps.

Output from PLL 3 goes through buffer amplifier Q14 (2SC2668) and is fed into the mixer in the main loop, where the signal is used to form the digital VFO signal. As a result, the operating frequency does not change even if the carrier frequency is changed, which

## CIRCUIT DESCRIPTION

into pin 2 of MIX5 IC7 (SN16913P) via the LPF. In MIX5, the signal is mixed with the signal generated by PLL4 and goes through the BPF to generate a signal in the range of 6.53 MHz to 6.6301 MHz (in 100 Hz steps). The generated signal is supplied to pin 5.

### • PLL2

PLL2 consists of IC9 (MN6147) and its loop circuitry. VCO2, Q18 (2SC2668), is locked in the range of 58.25 MHz to 53.2501 MHz. The 9 MHz reference frequency signal is supplied to pin 3 of IC9, where the signal is divided by 450 to generate a 20 kHz signal for frequency comparison. VCO2's output goes through buffer amplifier Q19 (2SC2668), and is fed into MIX4 pin 2 and mixed with the 6.35 MHz to 6.63 MHz signals applied to pin 5. The mixed signal then goes through the BPF to obtain 64.78 MHz to 59.88 MHz signal (in 100 kHz steps). The 64.78 MHz to 59.88 MHz signal is fed into IC9 pin 16 via buffer amplifier Q15 (2SC2668). In IC9, the signal is divided by M, and the phase of signal is compared with that of the 20 kHz reference signal by the phase comparator, and thus MIX4 output is locked (in 100 kHz step). The division ratio M is supplied from the digital unit (DA0 to DA3 and CK1), and is in 50 steps from 3239 to 2994 corresponding to 0.00 MHz to 0.49 MHz.

The output from PLL2 goes through buffer amplifier Q20 (2SC2668) and is divided by ten in IC10 (M54460L). Via the LPF, the signal is fed into pin 2 of MIX3 IC11 (SN16913P). The frequency of the signals depends on the values of L and M, and is in the range of 5.825 MHz to 5.32501 MHz (10 Hz step).

VR1 in MIX4 circuit is used to suppress spurious outputs from the mixer. It is necessary to prevent PLL2 from becoming unlocked.

Signals generated by PLL2 and the 9 MHz reference frequency are mixed in MIX3. The mixed signal goes through the BPF, and is further mixed with  $f_{L0}$  in MIX2 IC12 (SN16913P) on the IF unit. The output from MIX2 goes through the BPF to obtain 38.55 MHz to 39.04999 MHz. The signals are then mixed with the output from the final VCO oscillator in MIX1.

### • PLL1

The last PLL loop, PLL1, consists of IC17 (MB87006) and its loop components. In IC17, frequency division for reference and comparison frequencies is set by serial data (SO, SCK, and LE). When an external prescaler is used, IC17 has a modulus control function for configuring the pulse swallow counter.

The VCO oscillator output from the RF unit goes through Q26 (2SC2668) in the PLL unit and is fed into MIX1. The mixed signals go through the BPF, and they are then amplified by buffer amplifiers Q27 thru Q30 (2SC2668), shaped by IC15 (SN74S10N1/3), and fed into IC16 (WN74S112N) 1/3, or 1/2 prescaler. Basically, IC16 is a two-level FF circuit and functions as a 1/4 divider. But, when IC17 of the PLL unit sends control signals, to IC16, IC16 functions as a 1/3 or 1/2 frequency divider in con-

The 9 MHz reference frequency signal is supplied to pin 1 of IC17, where the signals are divided by 18 to generate a 500 kHz signal for frequency comparison. Signals fed into IC17 pin 8 via MIX1 and the buffer amplifier are divided by N, and the phase is compared with that of the 500 kHz reference signals by the phase comparator. The signal then goes through the active LPFs Q31 to Q33 (2SC2459) and is fed into the RF unit as VCO voltage signals to control the variable capacitor of the final VCO. The frequency divider N covers the full range of operating frequencies from 30 kHz to 30 MHz (500 kHz step), and it has 61 steps of frequency division data supplied by the microprocessor in the digital unit.

The last VCO signal in PLL1 therefore depends on the values of L, M, and N, and it is in the range from 45.08 MHz to 75.05 MHz (10 Hz step). N is expressed as follows:

$$N = PN_0 - A \\ (N_0 > A)$$

P: Prescaler module value

No: Programmable counter value

A: Swallow counter value

PLL IC contains  $N_0$  and A.

The last VCO unit is contained in the RF unit and consists of four VCOs, each handling one portion of frequencies from 30 kHz to 30 MHz. The appropriate VCO is selected by the microprocessor according to band information from the digital unit.

### • Unlock

If a PLL loop enters a unlock state, the output on the UL pin becomes L. This L signal is sent to the digital unit to stop the microprocessor.

### • 500 kHz marker signal

The 500 kHz reference signal for frequency comparison is supplied from IC17 pin 13, and it is used as the marker reference signal.

## 5. Digital control circuit

The TS-440 digital control circuit uses an 8-bit CPU (7800) which does not contain ROM, and has a 16K ROM (27128) and a 2K RAM (8418) outside the CPU. A common bus used for data exchange between the CPU and RAM, and between the CPU and ROM and is also connected in parallel to the two 8255's for extended I/O and an 8251 for interface to a personal computer (option). To transfer data to or from an appropriate IC, the CPU uses the WR or RD signal, and the chip select signal from the 74LS138.

The display is dynamically controlled by software, and consists of 13 digits and nine segments. The 13 digit and seven segment signal is driven by the high voltage resistive buffer (6300), and the other two segment signals are driven by a transistor. The 7800 transfers data serially. The clock signal

## CIRCUIT DESCRIPTION

pulses and U/D signals from two clock signals which are 90° out of phase with each other, and sends the pulses and signals to the 7800. A clock pulse interrupts the 7800 and a U/D signal causes the 7800 to perform a count up or down operation for each step. If fast rotation occurs, the 7800 processes several steps of PLL data at one time.

Voltages from the RIT and IF shift VRs are converted from analog to digital by the A/D converter IC (4052) and fed into the 7800. The voltages are used to drive the display and are reflected in the PLL data.

The digital control circuit contains two 8255's for extended I/O. The 8255 in control unit A is an output only element and the 8255 in control unit B is an input only element for key scan and static data. The output 8255 emits VS-1 signals,

PLL data for the 6147, clock signals, and 1 MHz LED data. The input 8255 receives key scan data such as panel switch data and DIP switch data for CAR compensation. It also receives static data which cannot be entered as a portion key scan data.

The 7800 outputs four bits of band and mode information (11 bands in the frequency range from 30 kHz to 30 MHz). Each time the 8251, used as the interface to a personal computer, receives one byte of data, the 7800 is interrupted and reads the data from the 8251. The 7800 analyzes any command in the data. In response to the command, the 7800 controls setting or writes data to the 8251 as required. The 8251 serially sends one byte of data including a start bit, synchronizing to a 4800 Hz clock signal.

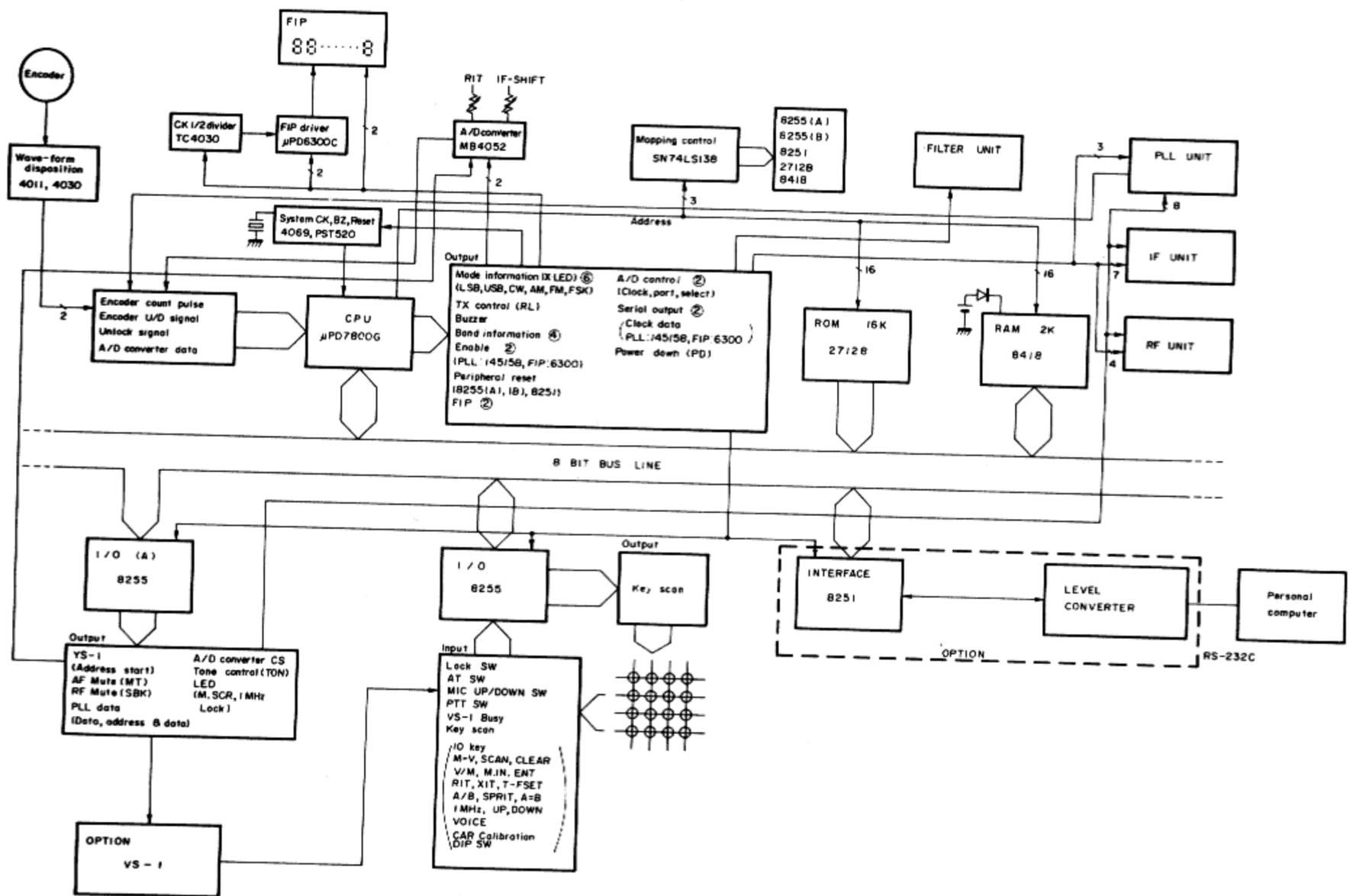


Fig. 13 Control circuit block diagram

# CIRCUIT DESCRIPTION

## 1. Encoder

The TS-440S uses an optical encoder. Two different clock signals from the encoder are 90°, out of phase with each other. This phase difference is not adjustable but depends on the precision of the module. The two clock signals are

converted into clock pulses (250 pulses/rotation × 4) and U/D signals indicating the direction of rotation by the 4011 and 4030 and fed into the 7800. Figure 15 is a timing chart for clock pulse and the U/D signal transmitted to the 7800.

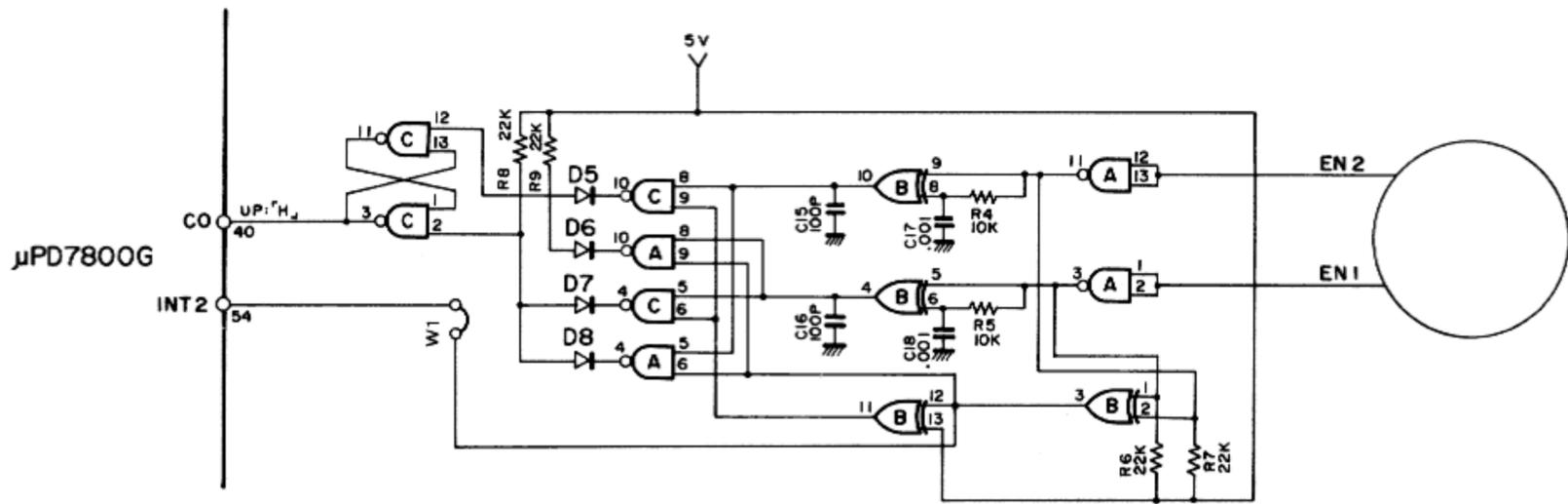


Fig. 14 Encoder circuit

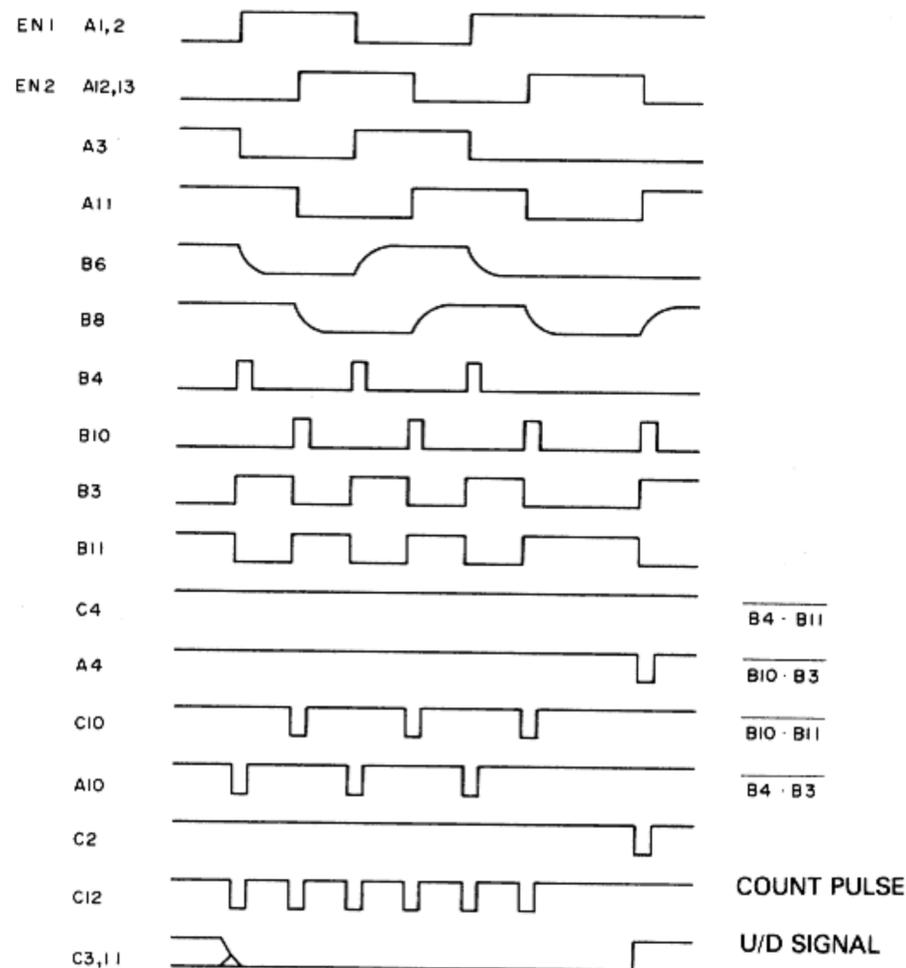


Fig. 15 Encoder waveform timing chart

## CIRCUIT DESCRIPTION

### 2. Digital display

FIP digit and segment signals are driven by the 6300 but decimal point and red character signals are driven by a transistor. 8 V is used to increase the brightness of red characters. The 7800 sends display data serially at 1 MHz, but the clock signals are divided by two (500 kHz) in the 4080 and fed into the 6300. Figure 16 shows how the frequency division is accomplished. The 7800 sends data from its SO pin

(pin 28) and a clock signal from its SCK pin (pin 26) at approx. 1 ms intervals. After the 7800 has sent 8 bits of data five times, the 7800 sends a negative enable pulse from port B5 (pin 46). When a decimal digit goes on, the 7800 sets port C4 to L and when a red character goes on the 7800 sets port C3 to H.

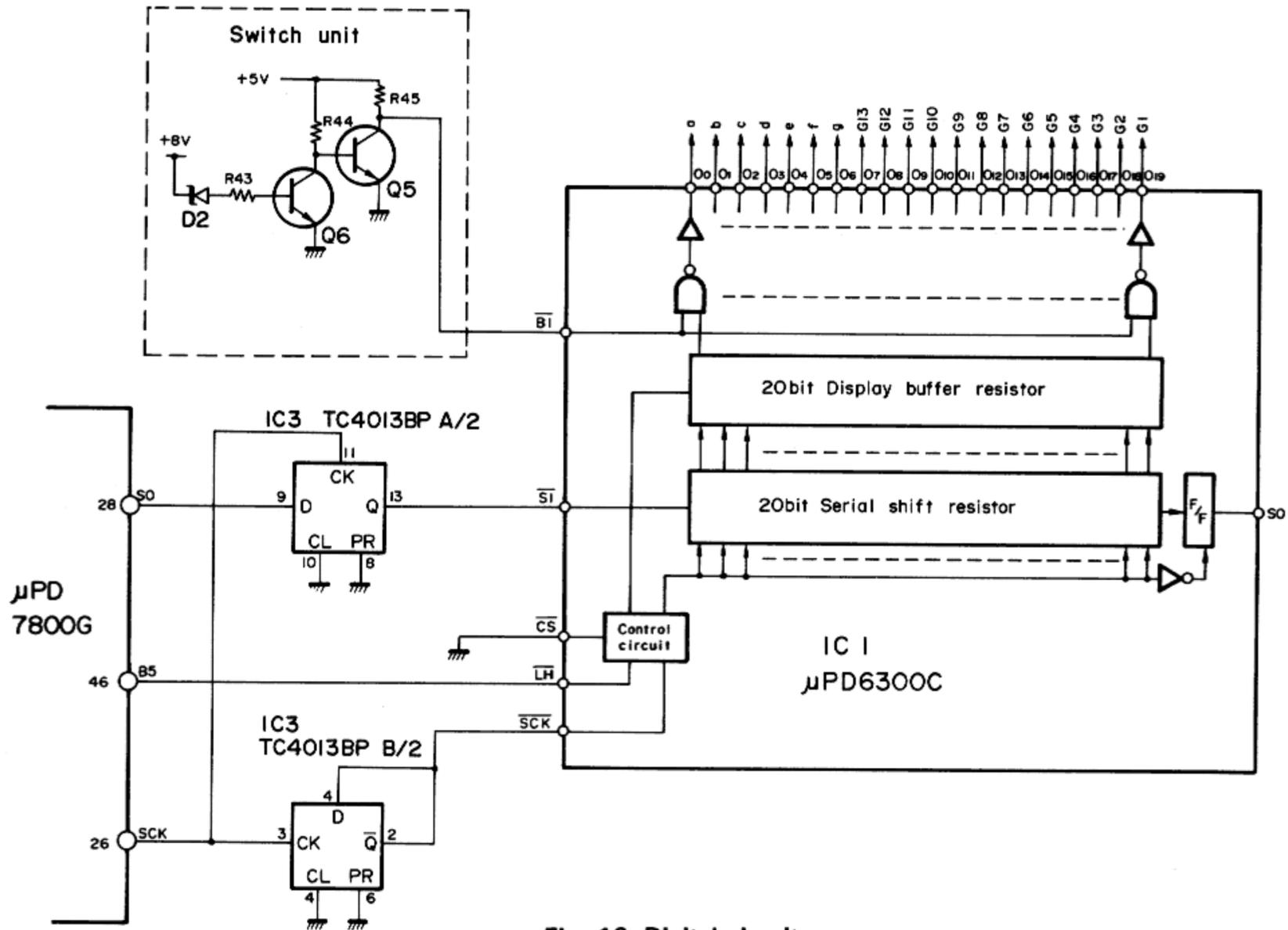


Fig. 16 Digital circuit

### 3. Key scan input

The key scan input block sends key scan signals (negative pulses) from its 8255 (IC53) port C in the order of C0 to C7 (C6 and C7 are output only once when the POWER switch is turned on). When a matrix crossing point switch is on, its

corresponding bit in the 8255 port A is L to enable the switch to be identified. Figure 13 shows the matrix. Key scan S6 and S7 are provided for the extended function using diodes.

Key scan matrix		S											
		1		2		3		4		5		6	
K	1	1	LSB	2	USB	3	CW	4	AM	5	FM		
	2	6		7		8		9		0	FSK		
	3	V/M		M·V		SCAN		M·IN		CLEAR		ENT	
	4			RIT		ZIT		T-FSET		1MHz		DOWN	
	5			A/B		SPRIT		A = B		25L	1	U.P	
	6	VOICE		T.SET ON		CLOCK 1		100L	3	50L	2	100U	8
	7	T.SET OFF						200L	4	25U	6	200U	9
	8	TIMER		SET		CLOCK 2		400L	5	50I	7	400U	10

## CIRCUIT DESCRIPTION

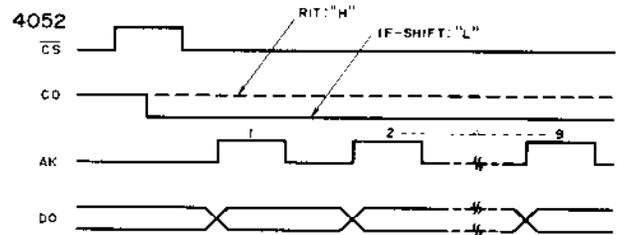
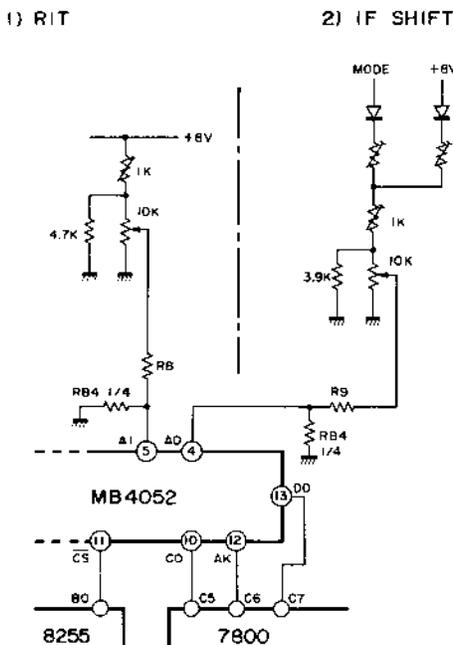
### 4. Static input

7800 (IC1)		
C0	Encoder U/D signal	"H" when UP
C2	Unlock signal	"L" when unlock
07	4052 (IC: Display)	A/D convertor data
8255 (IC53)		
B0	Lock switch	"L" when switch on
B2	AT switch	"L" when switch on
B3	MIC UP switch	"L" when switch on
B4	MIC DOWN switch	"L" when switch on
B5	PTT switch	"L" when switch on
B7	VS-1 busy signal	"H" when VS-1 busy

Table 11.

### 5. A/D convertor input

Voltages controlled by the RIT and IF shift VRs are applied to the 4052 (IC2: Display). The 4052 has four analog inputs: A0 (IC2 pin 4) is connected to the IF shift VR, and A1 (pin 5) is connected to the RIT VR, the other two inputs are not used. When reading IF shift data, the 7800 sets port C5 to 0 and selects 4052 A0. As a result, the 3255 sends a positive pulse from port B0 to reset the 4052, and the 7800 sends nine positive pulses from port C6, and port C7 receives data. When reading RIT data, the 7800 sets C0 from the 4052 to H and thereafter performs the same operations as when reading IF shift data.



A/D converter Input  
Fig. 17 A/D converter circuit

### 6. AT control

When the AT switch is turned on with the AUTO/THRU switch in the AUTO position, 8255 (IC53) ports B2 and B5 go on. When the 7800 knows that the AT switch is on via port B2, it will enter the CW-mode, and sets port A2 to H and A0, A1, and A3 to A6, and B4 to L, and transfer a power down signal. The 7800 then knows that the PTT switch is on via 8255 port B5, and sets port A6 (transmission control signal) to H, enabling transmission. However, if the selected frequency does not allow the 7800 to prepare for transmission, 7800 port A6 remains L and the 7800 will not enable transmission. When the selected frequency is 1.9 MHz or less, the 7800 will not enter CW mode nor send a power down signal.

### 7. LED output

Depending on the mode, the 7800 makes the 8255 (IC2) send M, SCR, 1 MHz, and lock LED signals from ports B4, B5, and B6. When the LED goes on, these ports are L. When the mode LED is on, 7800 ports A0 to A5 are H. A0 to A5 correspond to LSB, USB, CW AM, FM, and FSK respectively. Mode LED output is used as mode control signals in the IF unit.

### 8. VS-1 (option)

When the voice switch is turned on, an address corresponding to the instruction (numerical data) entered is sent from 8255 (IC2) ports A0 to A4 and a positive start pulse signal is sent from port A5. The VS-1 sends busy signals (H) to 8255 (IC53) port B7 while the voice switch is on. After the voice switch goes off, an address corresponding to the next instruction and a start signal are sent.

### 9. $\mu$ PD 7800 reset circuit

The 7800 reset circuit is used to initialize the 7800 when the POWER switch is turned on. This circuit supplies a reset pulse to the 7800 after the clock is supplied to the 7800 system clock input, X1 (pin 31). Since IC3 remains on until PST520D (IC3) pin 1 reaches 4.3 V, C10 is not charged, enabling a reset signal to be supplied. When pin 1 exceeds 4.3 V, IC3 goes off, causing C10 to charge via R2 and R3 and the reset signal is removed.

## CIRCUIT DESCRIPTION

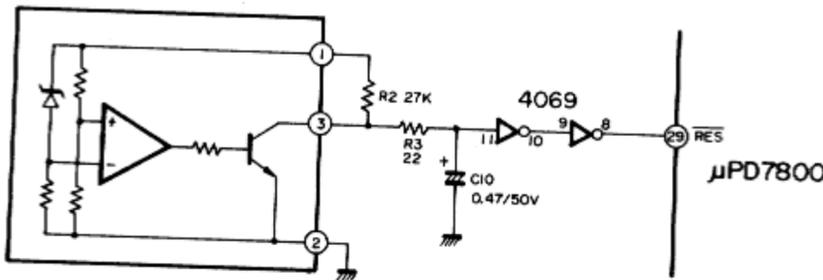


Fig. 18 Reset circuit

### 10. PLL output block

The PLL output block controls five PLL loops. The 500 kHz step PLL loop uses an MB87006 and the other PLL loops use MN6147s.

The M387006 has two dividers: one for the PLL reference frequency and the other for a swallow type counter. Frequency division data for the reference frequency is sent only one when the TS-440 power is switched on.

The MN6147 uses the PLL data format shown figure 19.

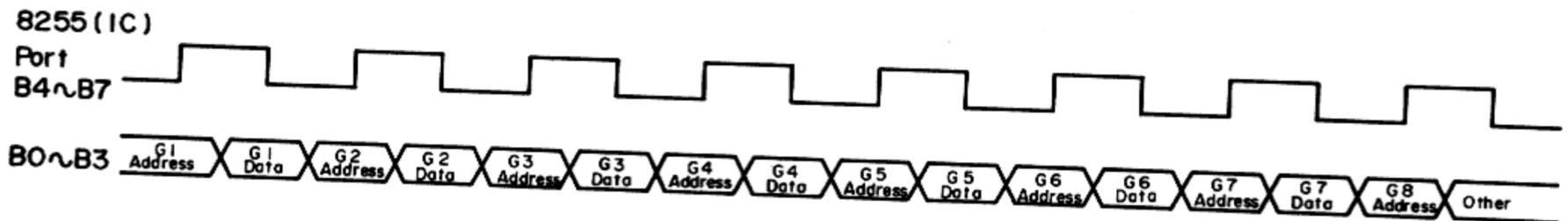


Fig. 19 MN6147 PLL data

Since the MN6147 has latches as shown in Figure 20, only data following a change is output. G0 data can be any data since it is used to transfer G2 and G7 data to the G8 latch.

### 11. Other outputs

#### RL output (7800 port A6)

This output signal controls transmission. When transmitting, this signal is "H".

#### BZ (Buzzer) output (7800 port A7)

This output signal makes the BZ circuit active. When this signal is "H", the oscillator circuit operates.

#### RESET output (7800 port B7)

This output signal resets the two 8255s and 8251 (option).

#### SBK output (8255 (IC2) port A6)

This output signal switches the RF unit to prevent noise due to PLL switching.

#### MT output (8255 (IC2) port A7)

This output signal controls the AF output to prevent noise due to PLL switching.

#### SCH output (8255 (IC2) port C0)

This signal controls the sub audible tone encoder. The sub-tone is activated whenever a transmit frequency in M-CH 90-99 has been selected, in the FM mode. A logic H activates the encoder.

### 12. CAR compensation DIP switch

This switch is used to compensate the absolute frequency characteristic of the 455 kHz filter. The characteristic can be compensated within the range of -400 Hz to +375 Hz. LSB and USB can be compensated separately. When LSB is compensated, FSK is also compensated.

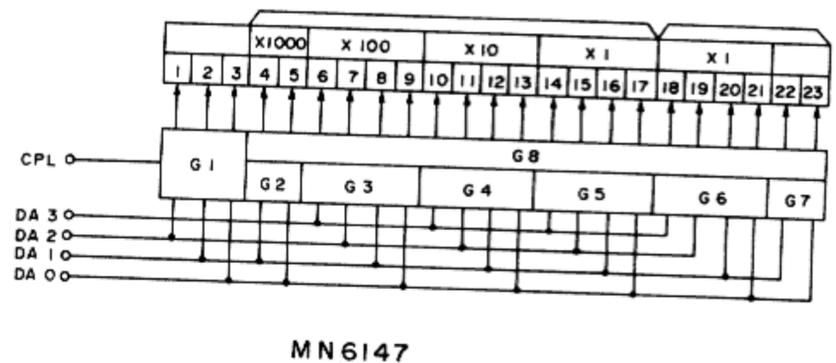


Fig. 20 Data input terminal and programmable counter

SW No.	Hz	
1	25	LSB
2	50	
3	100	
4	200	
5	400	
6	25	USB
7	50	
8	100	
9	200	
10	400	

Table 12

When all bits are off, -400 Hz is supplied for compensation. When no compensation is required, bits 5 and 10 must be set to 1.

### CIRCUIT DESCRIPTION

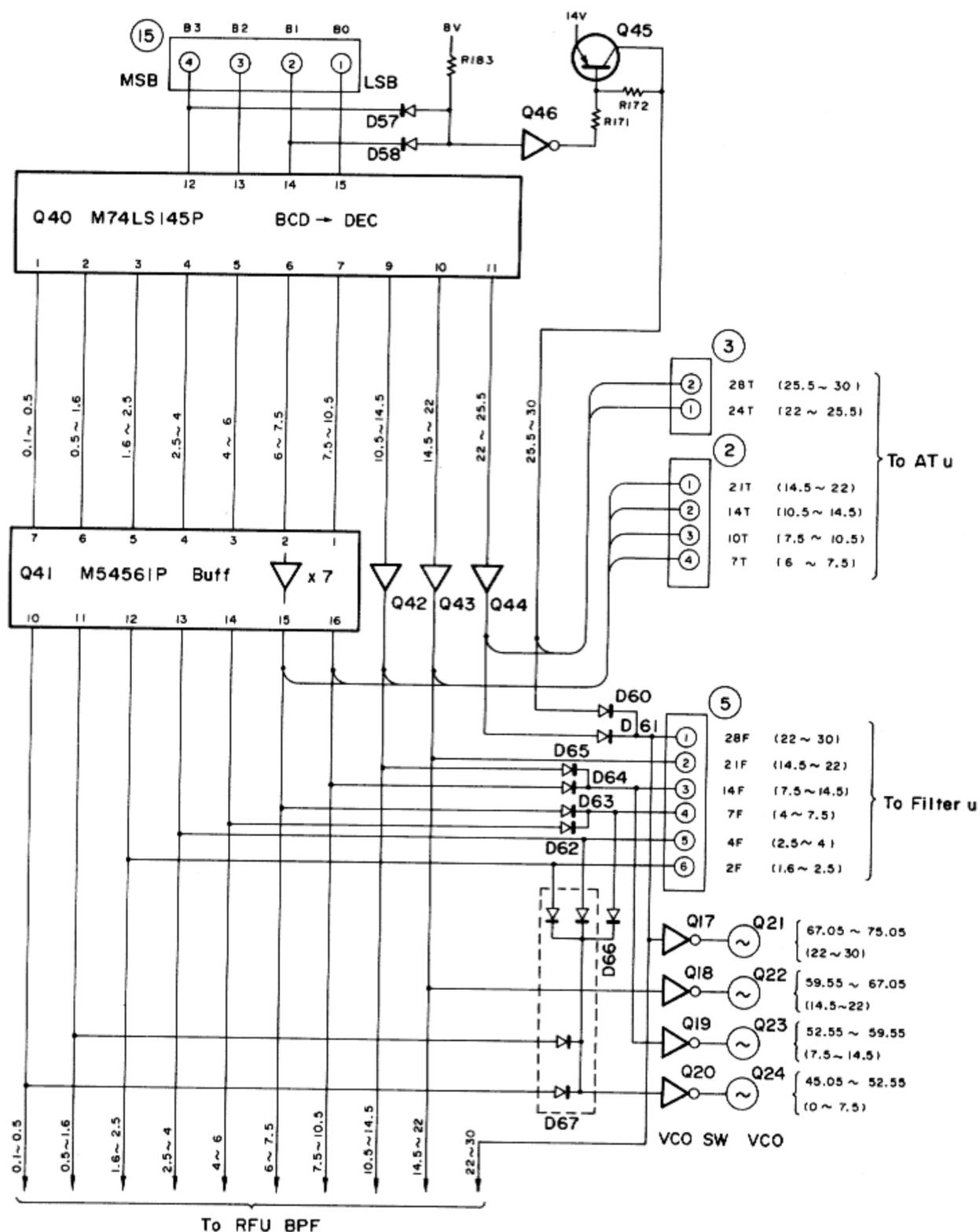
#### 13. Band information generation circuit (in the RF unit)

Band information from the control unit is sent to connector 15 of the RF unit. Band information signals B0 to B3 form a BCD code in which B0 corresponds to LSB. Q4D (M74LS145P) is used to convert data from BCD to DEC, and it generates control signals for ten of the 11 bands. Control signals for the remaining band (25.5 MHz to 30 MHz) are generated in the AND circuit consisting of D57, D58, and Q46. These control signals go through the current buffer consisting of Q41 to Q45 (M54561P and 2SA562Y), and are OR'ed by diodes, as required, and sent to AT unit, filter unit, CO, and ANT BPF, as shown in Figure 21.

Band information 7800 PB<sub>0</sub> ~ 3, B<sub>3</sub>B<sub>2</sub>B<sub>1</sub>B<sub>0</sub>

30kHz ~ 0.5MHz	0000
0.5MHz ~ 1.6MHz	0001
1.6MHz ~ 2.5MHz	0010
2.5MHz ~ 4MHz	0011
4MHz ~ 6MHz	0100
6MHz ~ 7.5MHz	0101
7.5MHz ~ 10.5MHz	0110
10.5MHz ~ 14.5MHz	0111
14.5MHz ~ 22MHz	1000
22MHz ~ 25.5MHz	1001
25.5MHz ~ 30MHz	1010

Table 13



## CIRCUIT DESCRIPTION

### 14. Mode control signals

Transmit/receive mode signals are generated by IC10 in the IF unit. IC10 is a hybrid IC containing five pairs of PNP transistors and diodes.

Figure 22 shows its equivalent circuit. When the mode signals SSB, CWB, RYB, AMB, and FMB are applied to pins 6

to 10, the voltages of control pins 16 and 17 change. During reception, these signals change to SSR, CWR, RYR, AMR, and FMR. During transmission, these signals change to SST, CWT, RYT, AMT, and FMT.

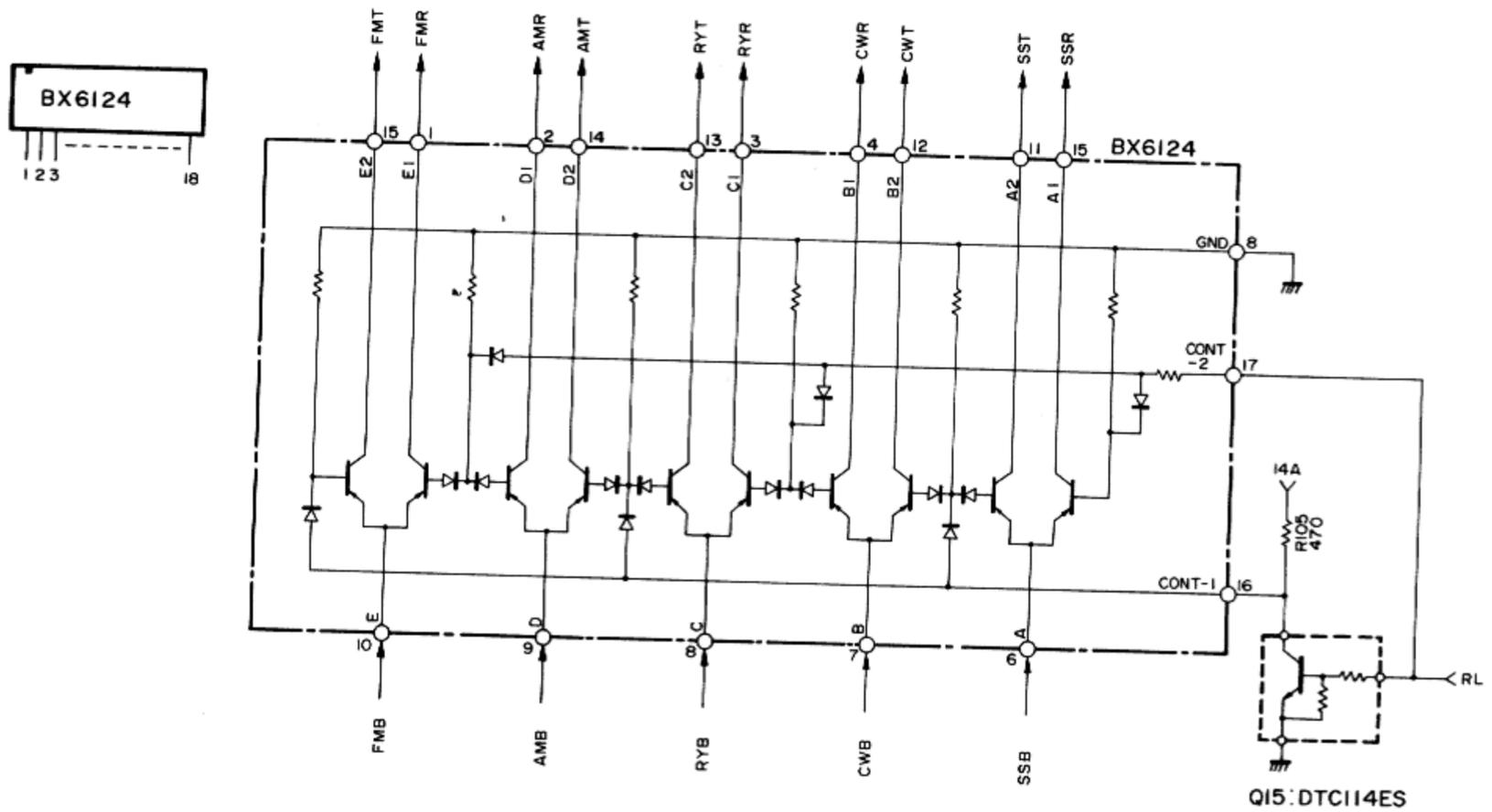


Fig. 22 Mode control circuit

### 15. Expand function

Control unit (X53-1450- 11 )

D No.	Shipped		Diode cut
65	Mode beep tone	Morse	Single tone
66	10Hz display	OFF	ON
67	Memory protect	OFF	ON
73	CW shift	800Hz	400Hz
78	W 24 TX	No	Yes
79	W 18 TX	No	Yes

Table 14 Expand function

## 16. Semi-self test function

Semi-self test is started by turning the POWER switch on with the **4** (AM) and T-F SET switches pressed.

This test provides a method of testing the TS-440 digital system in a shorter time during production or servicing. The test enables the following:

1. Circuits which are difficult to test during program execution to be tested easily. For example, dynamic data can be output as static data.
2. Items on which information is held only by the CPU and is not available to the user to be tested.

- a. Approximately threshold level input
- b. Incorrect input due to input pin fault

### Operation procedure

1. POWER SW OFF
2. The power switch on while pushing switch **4** (AM) and switch T-F SET
3. The test number has starts from "0" to "56" and END when turn the VFO knob clockwise. Operation chart shows as follow.
4. To reset SEMI-SELF TEST function, Power switch OFF.

### TEST NO. LIST

TEST NO	Condition	TEST NO	Condition
0	Start All Fip's light's	31	RES = "H"
1	All Fip's light's (Segment)	32	.. = "L"
2	All Fip's light's	33	CO = "H" (A/D)
3	All Fip's OFF (digit)	34	.. = "L" ( " )
4	Each digit lights G1	35	AX = "H" ( " )
5	" G2	36	.. = "L" ( " )
6	" G3	37	8255 Port A all = "H" (IC2)
7	" G4	38	" " all = "L" (..)
8	" G5	39	8255 Port B all = "H" (..)
9	" G6	40	" " all = "L" (..)
10	" G7	41	8255 Port C C0 ~ C3 = "H" (..) C4 ~ C7 = "L"
11	" G8	42	" " C0 ~ C3 = "L" (..) C4 ~ C7 = "H"
12	" G9	43	8255 Port C all = "H" (IC53)
13	" G10	44	" " all = "L" (..)
14	" G11	45	LOCK,PTT,MIC,U/D,AT,VS-1(BUSY)check
15	" G12	46	[SIMPLEX] VS-1(BUSY)check
16	" G13	47	Key scan inport check
17	BZ ON	48	<b>1</b> (LSB), <b>6</b> ,V/M,VOICE (check)
18	BZ OFF	49	<b>2</b> (USB), <b>7</b> ,M/V,RIT,A/B (check)
19	Mode LED all ON	50	<b>3</b> (CW), <b>8</b> ,SCAN,XIT,SPRIT (check)
20	" all OFF	51	<b>4</b> (AM), <b>9</b> ,MIN,T-FSET,A = B,100L 200L 400L ( " ) ③ , ④ , ⑤
21	RL = "H"	52	<b>5</b> (FM), <b>0</b> ,(FSK),CLEAR,1MHz,25L 50L 25U 50U ( " ) ① , ② , ⑥ , ⑦
22	" = "L"	53	ENT,DOWN,UP, 100U 200U 400U ⑧ , ⑨ , ⑩
23	BAND all = "H"	54	-
24	" all = "L"	55	-
25	PD = "H"	56	END
26	" = "L"		
27	ENF = "H"		
28	" = "L" (immediatly)		
29	ENP = "H"		
30	" = "L"		

# TS-440S

## SW Monitor

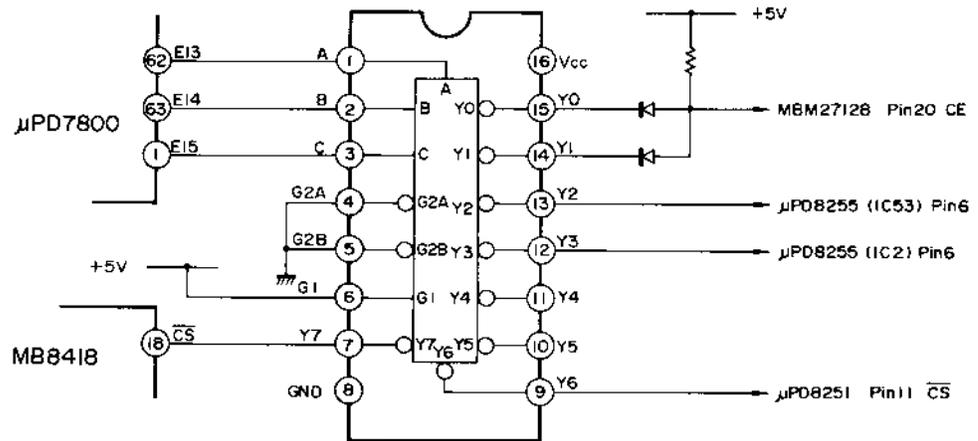
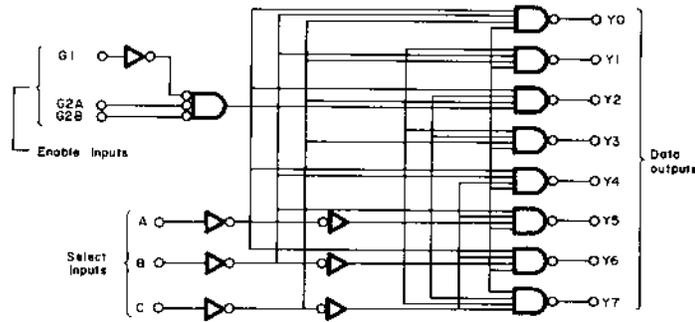
Display changes by TEST number

TEST NO	Display	/	/	/	/	/	/	/	0
45	LOCK			AT	MIC UP		MIC DOWN	PTT or AT	VS-1 BUSY
46									
47									
48	[1] LSB	[6]	V/M				VOICE		
49	[2] USB	[7]	M-V	RIT		A/B			
50	[3] CW	[8]	SCAN	XIT		SPRIT			
51	[4] AM	[9]	M.IN	T-FSET		A=B	100L ③	200L ④	400L ⑤
52	[5] FM	[0]	CLEAR	1MHz		25L ①	50L ②	25U ⑥	50U ⑦
53			ENT	DOWN		UP	100U ⑧	200U ⑨	400U ⑩

If the display changes from "/ " to " 0 " by operate the key in chart then function working properly.

SEMICONDUCTOR

SN74LS138H (Control unit IC51)



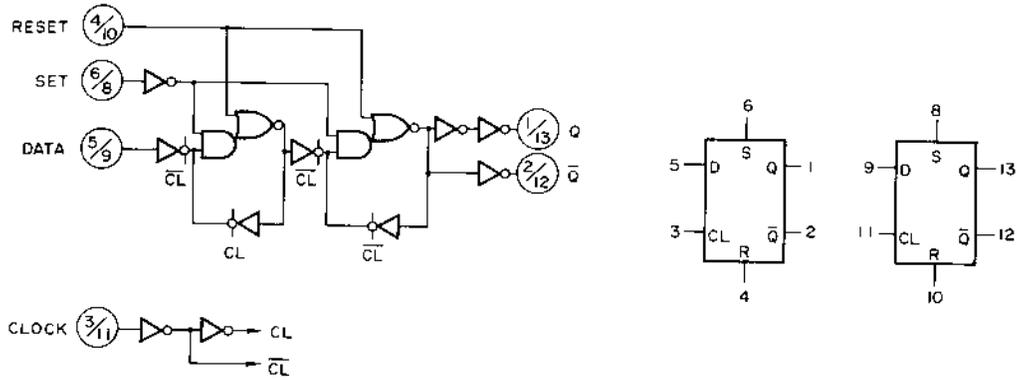
TRUTH TABLE

Input					Output							
Enable		Select			Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>	Y <sub>4</sub>	Y <sub>5</sub>	Y <sub>6</sub>	Y <sub>7</sub>
G <sub>1</sub>	G <sub>2</sub>	C	B	A								
x	H	x	x	x	H	H	H	H	H	H	H	H
L	x	x	x	x	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

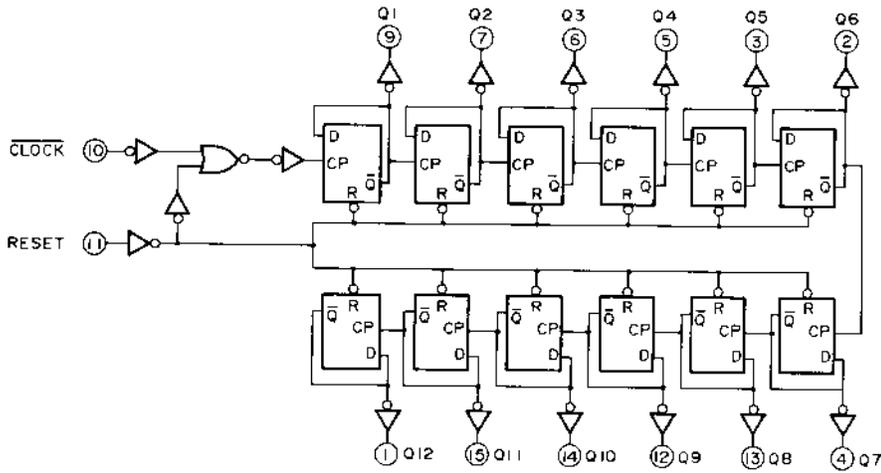
Note: 1.  $G_2 = G_{2A} + G_{2B}$   
 2. H: High level  
 L: Low level  
 X: "H" or "L"

## SEMICONDUCTOR

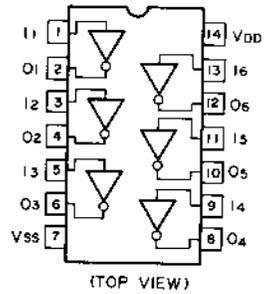
**TC4013 (Display unit IC3)**



**TC4040BP (Control unit IC55)**

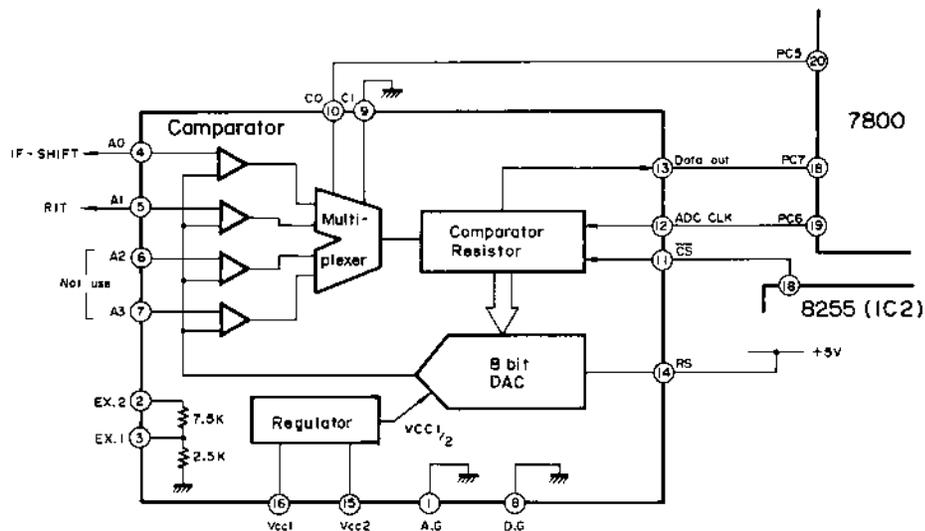


**TC4069BP (Control unit IC4)**



SEMICONDUCTOR

MB4052



MB4052 Pin Description  
I/O Signal Pin Functions

Pin No.	Pin Name	Symbol	Function
2	Range expander input	Ex. 2	Analog input pin for expanding the range.
3	Range expander output	Ex. 1	Analog output pin for expanding the range. Connect to any pin from A0 to A3. By using Ex. 1, Ex. 2, the range is expanded to the $\times 4$ range.
4 - 7	Analog entrance	A <sub>0</sub> - A <sub>3</sub>	4 ch analog input pin. Channel 1 is selected by channel select input C0 to C1.
9	Channel select input	C <sub>0</sub>	The input pin to designate the analog input channel for A/D converter. This signal is latched at the trailing edge of CS.
10	Channel select input	C <sub>1</sub>	
11	Chip select input	CS	This is the chip select input pin. When CS is inverted from "1" to "0", A/D converting starts and data output is enabled. After A/D converting is over or when an interrupt is required, set the CS back to "1".
12	A/D conversion clock	ADC CLK	This is the clock input pin for A/D conversion input to the comparator register sequentially. Conversion speed is determined by the clock speed. In the case of 8-bit, approx. 10 clocks will be needed. However, it is not necessary that the clock period be fixed.
13	Data output	DATA OUT	This is the open collector to output the result of A/D conversion. The data is output in the order of the start bit, most significant bit, 2nd significant bit, ..., least significant bit, and the stop bit, synchronized with ADCCLK.
14	Range select input	RS	This is the input pin for selecting the voltage range of analog input. The $VFS = Vcc_1/8$ range is selected at "0", and the range of $FVS = Vcc_1/2$ is selected at "1". During conversion, hold this pin to "0" or "1".
1	Analog ground	A.G.	Ground terminal
8	Digital ground	D.G.	
15	Power supply pin 2	Vcc <sub>2</sub>	When driving with 3.5 to 6.0 V of power, connect Vcc <sub>1</sub> and Vcc <sub>2</sub> to each other, and apply the power voltage to them. When driving 8 to 18 V of power, apply the power voltage to Vcc <sub>2</sub> . At this time, the 5 V stabilized voltage is output to Vcc <sub>1</sub> , and approx. 10 mA current can be supplied externally to the IC. When either 3.5~6.0 V or 8~18V power is used, Vcc <sub>1</sub> is the reference voltage for A/D conversion.
16	Power supply pin 1	Vcc <sub>1</sub>	

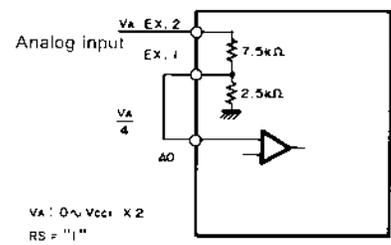
• Channel Select

C <sub>1</sub>	C <sub>0</sub>	Selected Ch.
0	0	A <sub>0</sub>
0	1	A <sub>1</sub>
1	0	A <sub>2</sub>
1	1	A <sub>3</sub>

• Range select

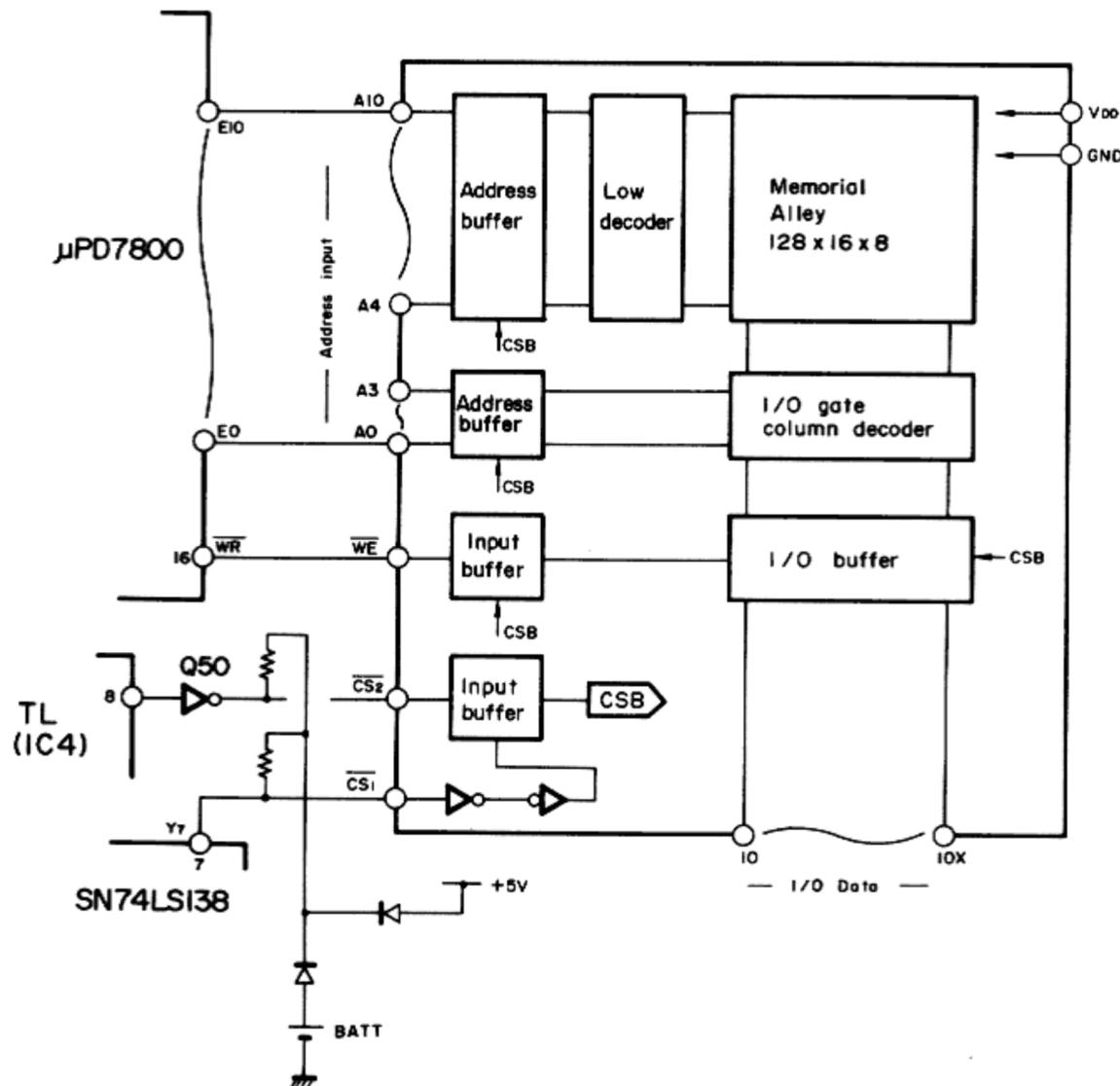
RS	Conversion voltage range
0	$0 \sim \frac{Vcc_1}{8}$
1	$0 \sim \frac{Vcc_1}{2}$

• Wiring example when expanding the range



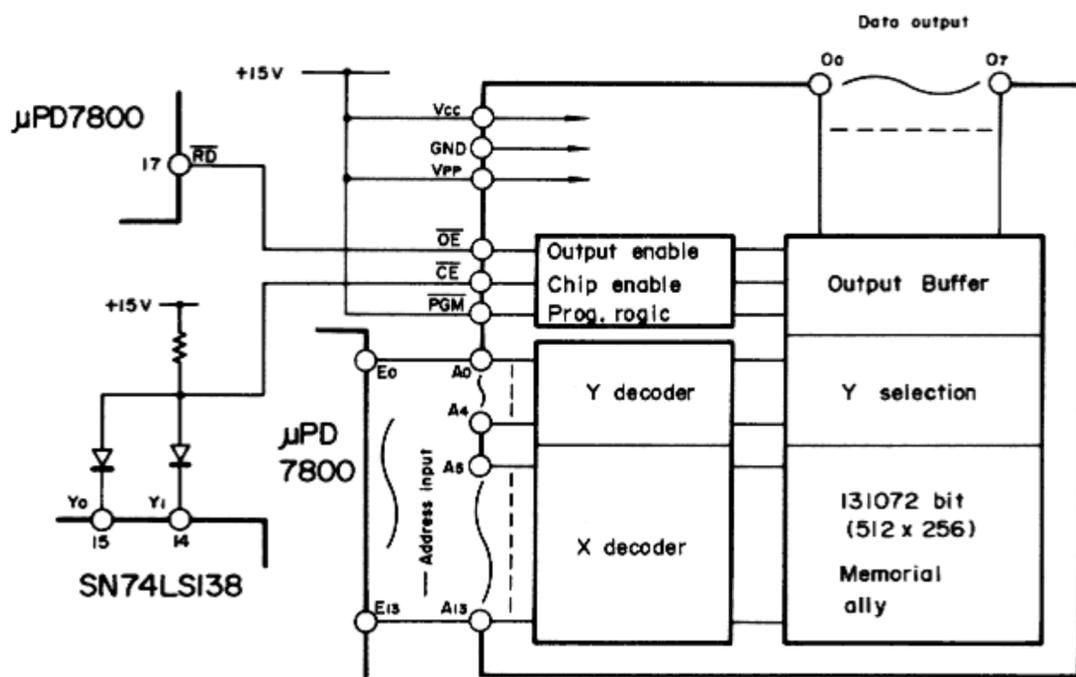
MB4052

MB8418-LP20-GRA (Control unit IC50)



Symbol	Pin name
A <sub>0</sub> ~ A <sub>10</sub>	Address input
I( ) <sub>1</sub> ~ I( ) <sub>X</sub>	Data in/out
$\overline{CS}$	Chip select 1
CS <sub>2</sub>	Chip select 2
$\overline{WE}$	Write enable
V <sub>cc</sub>	Power (1.5 V)
GND	GND
NC.	No connection

MBM27128 (Control unit IC52)

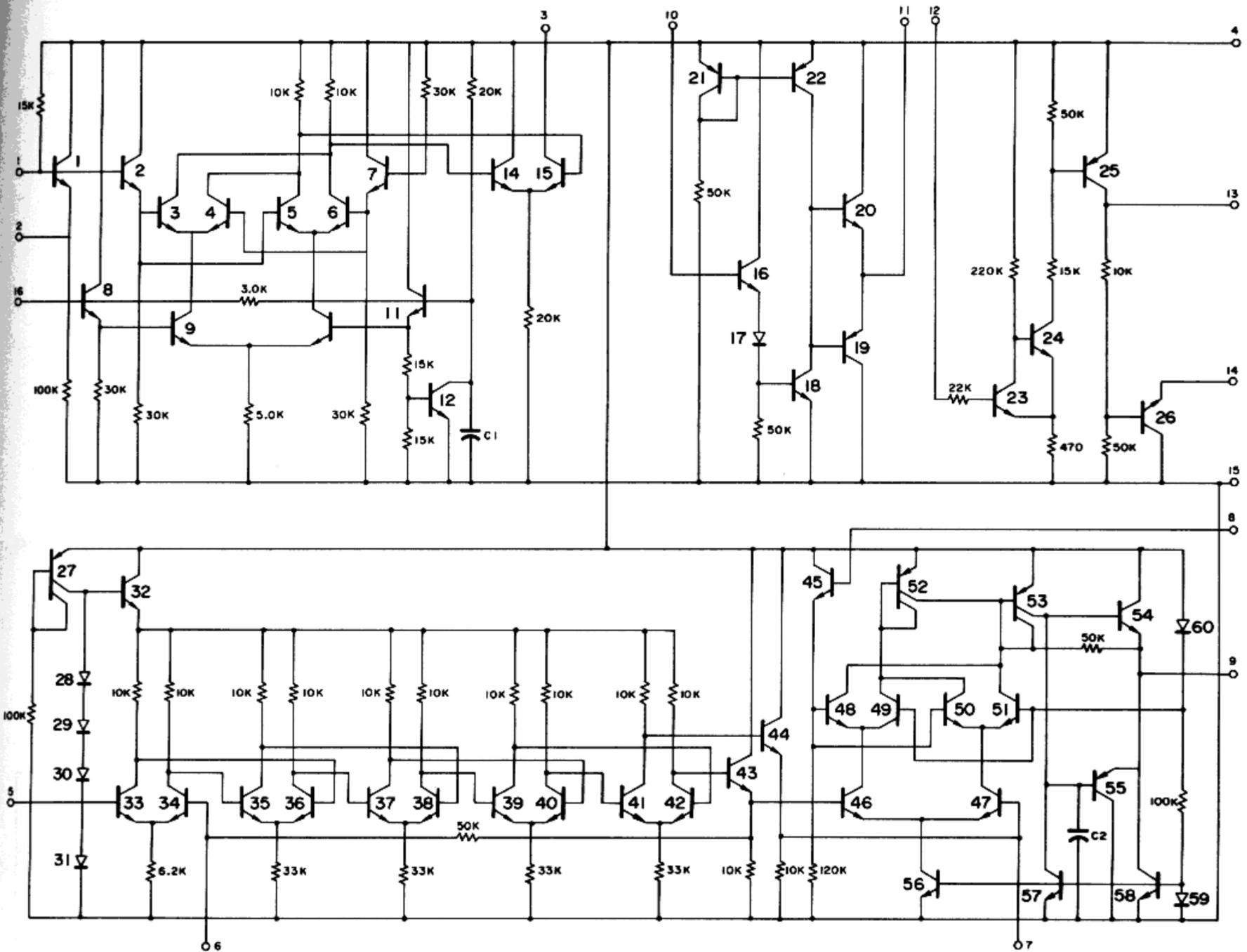


Pin name

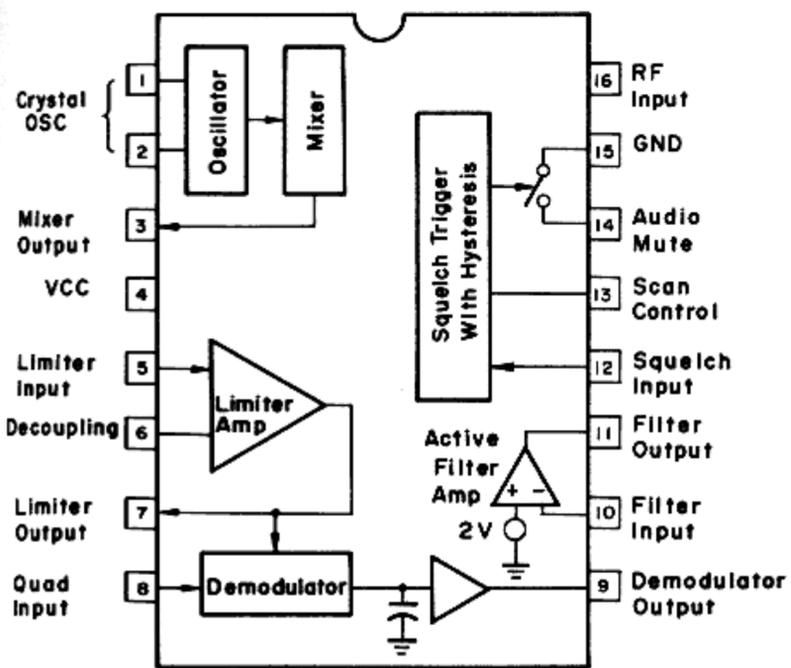
A <sub>0</sub> ~ A <sub>13</sub>	Address input
O <sub>0</sub> ~ O <sub>7</sub>	Data output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{PGM}$	Program input
V <sub>cc</sub>	Power supply
V <sub>pp</sub>	Program power supply
GND	GND

SEMICONDUCTOR

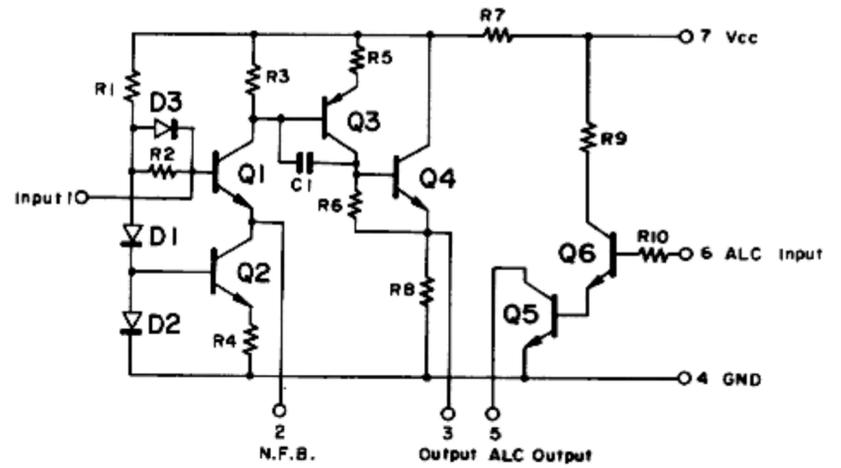
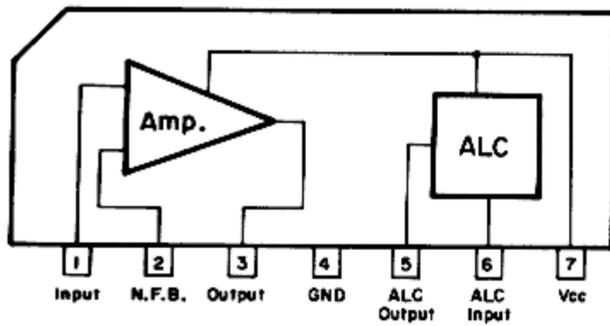
MC3347 (IF unit IC2)



MC3357 (IF unit IC2)



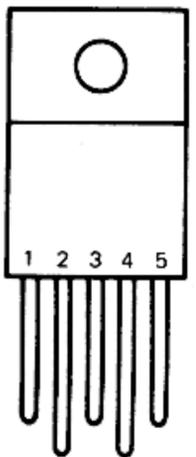
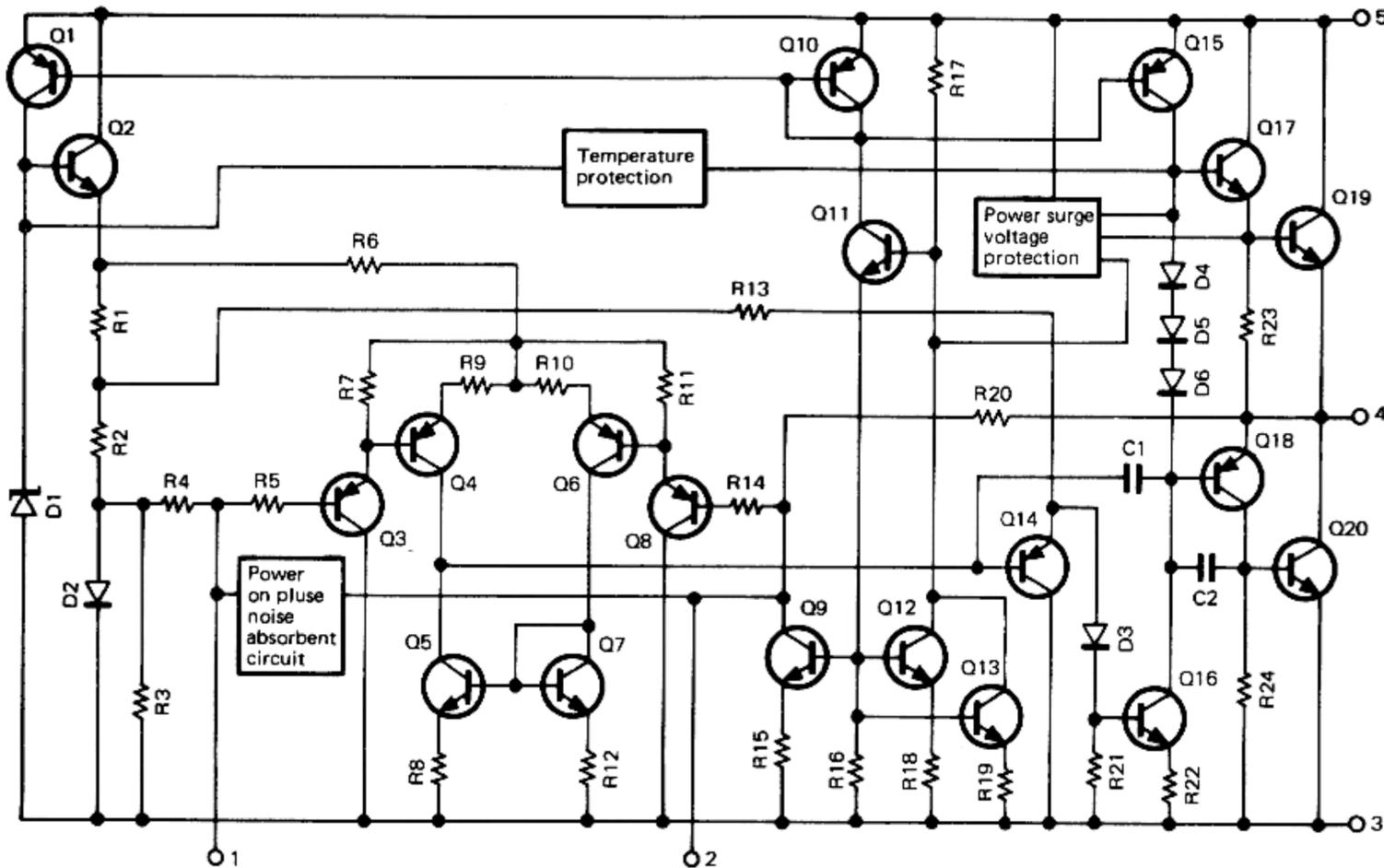
### μPC1158H2



#### Pin connection

Pin	Function	Pin	Function
1	Input	5	ALC output
2	N. F. B.	6	ALC Input
3	Output	7	Vcc
4	GND		

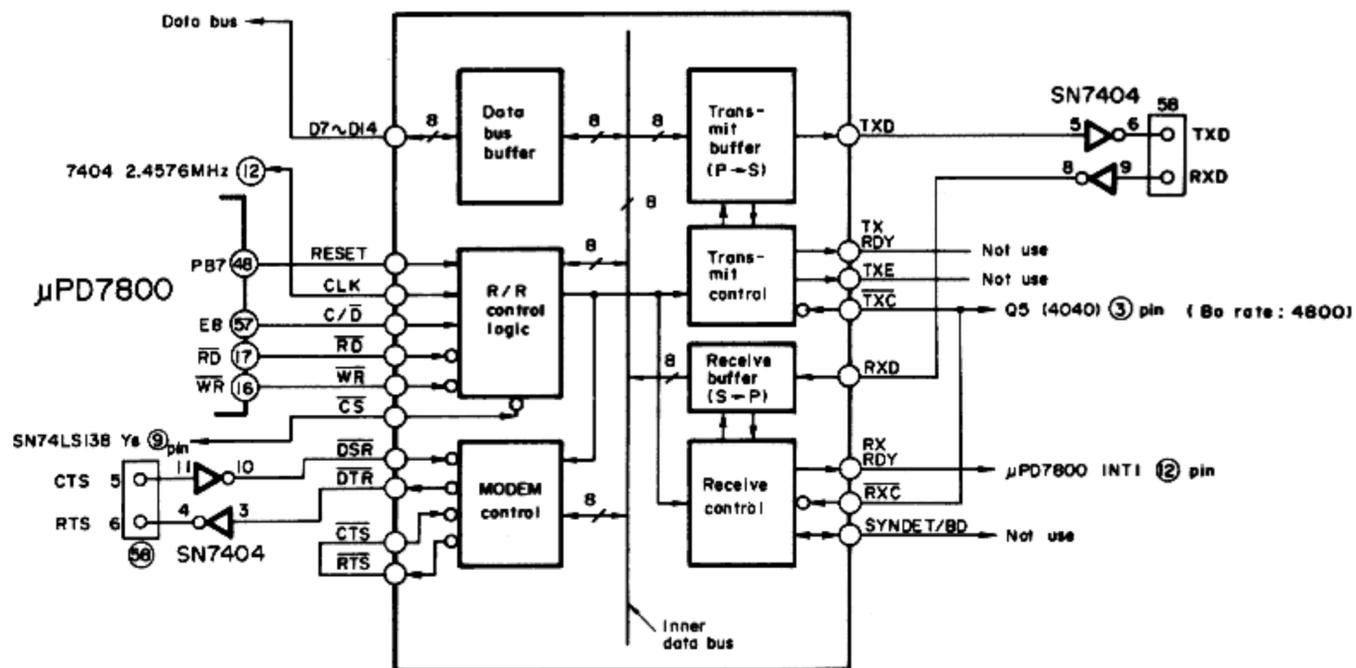
### μPC2002V (IF unit IC7)



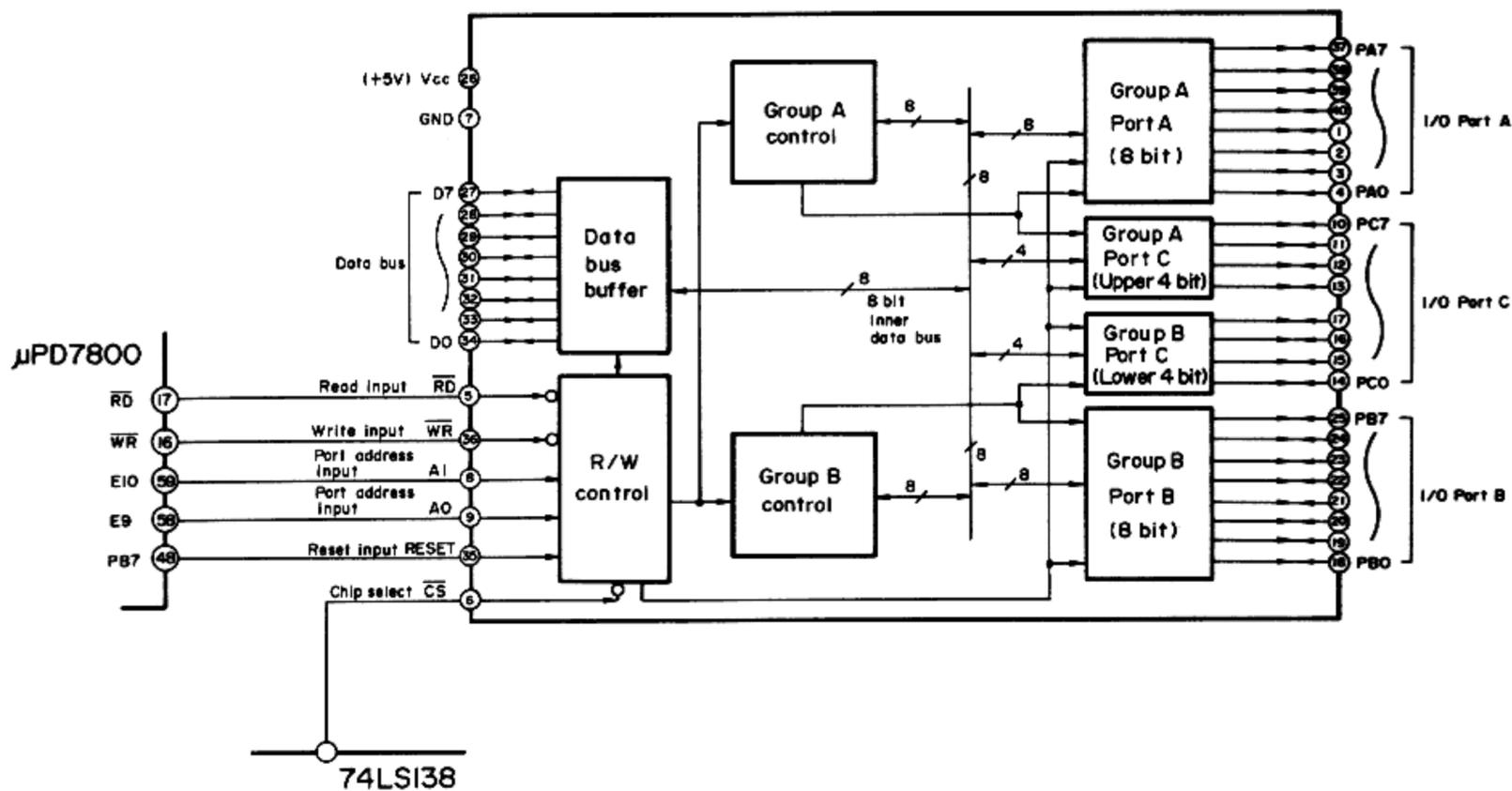
- 1 : Input
- 2 : NFB
- 3 : GND
- 4 : Output
- 5 : Power supply + Vcc

SEMICONDUCTOR

μPD8251AC (Control unit IC54)



μPD8255AC-5 (Control unit IC2, 53)



1) A1 IC2: Y3 (12)  
 1) A1 IC53: Y2 (13)

Basic function

A <sub>1</sub>	A <sub>0</sub>	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Function
0	0	0	0	1	Data bus ← Port A
0	1	0	0	1	Data bus ← Port B
1	0	0	0	1	Data bus ← Port C
0	0	0	1	0	Port A ← Data bus
0	1	0	1	0	Port B ← Data bus
1	0	0	1	0	Port C ← Data bus
1	1	0	1	0	Control register ← Data bus
x	x	1	x	x	Data bus is in high impedance status
1	1	0	0	1	Combination is inhibited

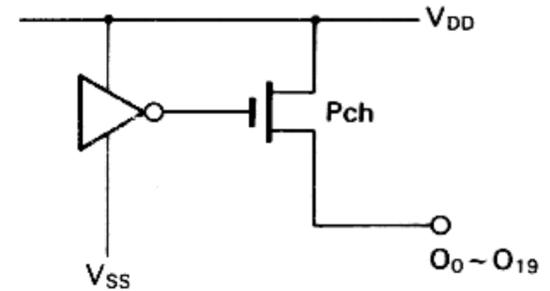
"0" shows low level (L)  
 "1" shows high level (H)

## SEMICONDUCTOR

### μPD6300C (Display unit IC1)

#### Pin description

Pin No.	Symbol	Pin name	I/O	Description
1 7	O <sub>13</sub> O <sub>14</sub> O <sub>15</sub> O <sub>16</sub> O <sub>17</sub> O <sub>18</sub> O <sub>19</sub>	FIP Segment driver (O <sub>13</sub> ~O <sub>19</sub> )	O	High dielectric-strength (40V) output in the Pch open. Corresponds to the output of O <sub>13</sub> ~O <sub>19</sub>
8	SO	Serial data output pin	O	Output serial data the trailing edge of SCK. When the n-number of μPD6300Cs are connected in series, this can be connected to the SI of the following stage.
9	$\overline{\text{BI}}$	Blanking pin	I	This input can turn off all indicator or displays, and can dim them by applying a random duty pulse from outside. Active low.
10	$\overline{\text{LH}}$	Latch pin	I	Transmits the connects of the serial shift register to the buffer register at low level, to latch the connects at the rising time. Active rising (leading) edge.
11	SI	Serial data input pin	I	This is the data input pin. Inputs data to the shift register at the rising edge of SCK.
12	$\overline{\text{SCK}}$	Serial clock input pin	I	Reads out the SI data to the shift register at the rising edge of SCK. Outputs data from SO at the trailing edge of $\overline{\text{SCK}}$ .
13	$\overline{\text{CS}}$	Chip select pin	I	When $\overline{\text{CS}}$ is high, this inhibits $\overline{\text{SCK}}$ and $\overline{\text{LH}}$ , and when $\overline{\text{CS}}$ is low, activates SCK and LH.
14	V <sub>SS</sub>	GND	—	Connect to the GND terminal of the system.
15 16 17 18 26 27	O <sub>0</sub> O <sub>1</sub> O <sub>2</sub> O <sub>3</sub> O <sub>4</sub> O <sub>5</sub> O <sub>6</sub> O <sub>7</sub> O <sub>8</sub> O <sub>9</sub> O <sub>10</sub> O <sub>11</sub> O <sub>12</sub>	FIP Segment driver (O <sub>0</sub> ~O <sub>12</sub> )		Pch open-drain system, high dielectric-strength output. Corresponds to the output of O <sub>0</sub> to O <sub>12</sub>
28	V <sub>DD</sub>	Power supply pin	—	5 V ± 10%















































































































































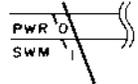






# ADJUSTMENT

Item	Condition	Measurement			Adjustment			Specification/Remarks
		Test equipment	Unit	Terminal	Unit	Part	Method	
	2) AT TUNE SW: OFF Disconnect No. 1 connector from AT unit. STBY: SEND Set. SWR 1.25 reading when VFO dial is turned.	Set as shown right.					Adjust VR2 until AT TUNE indicator just goes off.	
	3) STBY: REC AT TUNE: ON				AT	VR2		
	4) AF TUNE: OFF Reconnect No. 1 connector after adjustment.							









## ADJUSTMENT

### BOTTOM VIEW

