## *Tuner Unit*

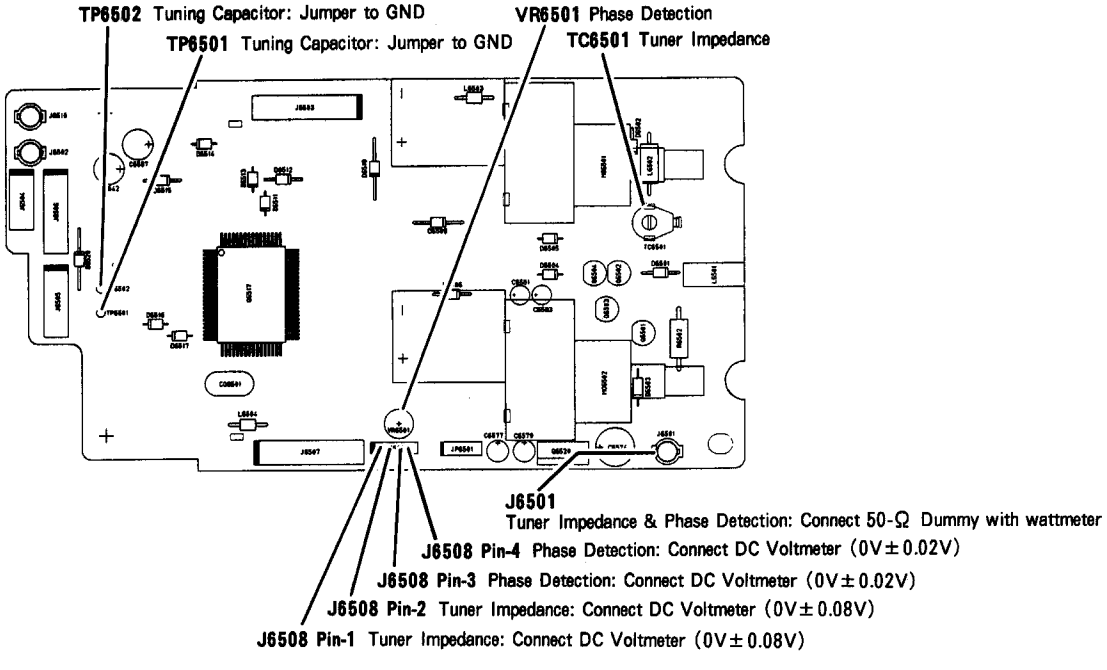
Refer to the photograph at the page bottom for TUNER Unit component locations and alignment points.

*Tuning Capacitor/Motor (Mechanical check, setting & adjustment)*

- ❒ Loosen all set screws in the shaft coupler, and turn the coupler by hand to confirm it moves freely (the motor and capacitor should not move).
- ❒ If the coupler binds, check the motor mounting position (it is soldered in place) and the capacitor mounting (screw).
- ❒ Turn the power switch off, and jumper TP6501 to chassis ground. Turn the power switch on The motor should rotate, and then stop.
- ❒ Set the capacitor to its maximum capacitance position (plates fully meshed) by hand, and tighten all shaft coupler set screws, using care not to disturb the capacitor or motor positions.
- ❒ Turn the power off, and jumper TP6502 to chassis ground (along with TP6501). Turn the power back on. The motor should move 180°, and the capacitor should be then at minimum capacitance (fully unmeshed). Remove the grounding jumpers from TP6501 and TP6502.

*Tuner impedance & Phase detection*

- ❒ Connect the 50-Ω dummy load and wattmeter to J6501 (the output of the Tuner-Control Unit), and connect J6502 (RF IN) to J5002 (LPF OUT). Select CW mode.
- ❒ Connect the DC voltmeter between pin-1 ("I") and 2 ("V") of J6508 (either polarity).
- ❒ Press the **TUNER** and **MOX** buttons, adjust the **RF PWR** control for 50 watts output, and then adjust TC6501, if necessary, for meter indication within ±0.08V of 0V.
- ❒ While still transmitting, move the DC voltmeter to pin-3 ("C") and 4 ("L") of J6508 (either polarity), and adjust VR6501, if necessary, for meter indication within ±0.02V of 0V.




**Tuner Unit Test & Alignment Points**

## IF Unit

Refer to the photograph at the page bottom for IF Unit component locations and alignment points.

### 2nd & 3rd Local Amp

❒ Connect the RF millivoltmeter to TP2003, and adjust T2010 for maximum indication on the RF millivoltmeter (at least 500 $mV_{RMS}$).

❒ Next, connect the RF millivoltmeter to TP2005, and confirm at least 100 $mV_{RMS}$.

### Rx IF Interstage Transformer (I) (coarse alignment)

❒ Connect the RF signal generator to J2003, and inject +100 dBu at 70.455 MHz. Connect the AC voltmeter across and 8-Ω dummy load to the **EXT SP** jack on the rear panel.

❒ Preset VR2004 12-o'clock position, and adjust T2003~T2009, T2011 and T2012 in succession several times for peak on the AC voltmeter.

### RF Interstage Transformers Coarse alignment

❒ Preset VR1002 and VR1003 to their 12-o'clock positions, and select either USB or LSB mode. Adjust T1015~T1019 on the IF Unit in succession several times for peak noise from the speaker.

### S-Meter Coarse Alignment

❒ Preset VR2003 fully counter-clockwise, and adjust VR2003 so that all S-meter segments are just off. Preset the **RF GAIN** control fully counter-clockwise, and adjust VR2002 so that all S-meter segments are just on.

### 1st Mixer Balance

❒ Preset VR1002 for 12-o'clock position.

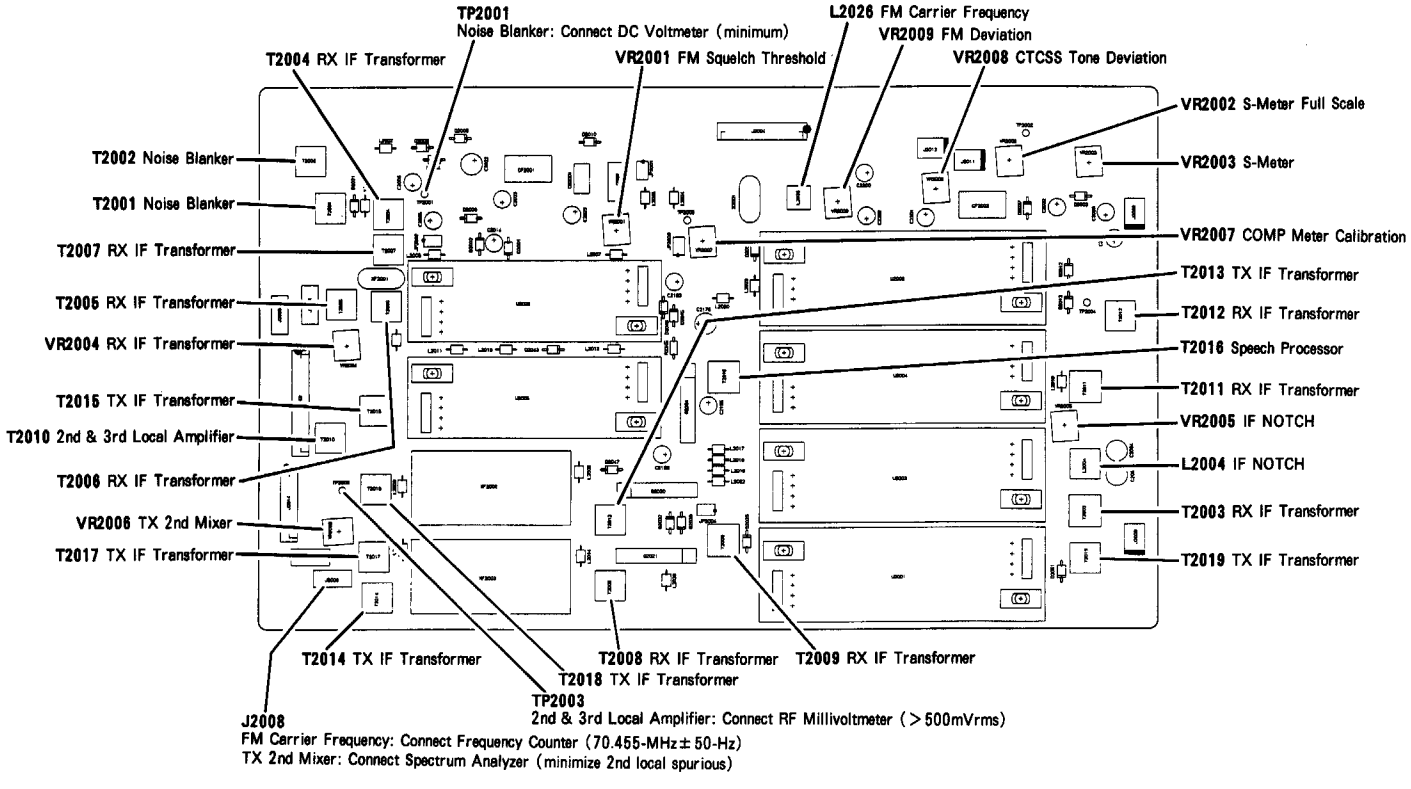
### IF Interstage Transformers (II)

❒ Connect the RF signal generator to the antenna jack, and inject a +80 dBμ signal. Adjust T1015~T1019, T2003~T2009, T2011 and T2012 in succession several times for peak S-meter indication (adjust the injection level as necessary to keep the meter around mid scale).

### RF Amp

❒ Confirm that menu function 8-4 is set to "tuned" then connect the RF signal generator to the antenna jack, and inject a +20 dBμ signal.

❒ Referring to the table at the top of the next page, tune the transceiver and RF signal generator to the listed frequencies, and adjust the corresponding components for the levels shown.




**IF Unit: Test & Alignment Points**

| RF Amp Alignment | | |
|---|---|---|
| **Tune SG & Radio to:** | **Adjust/Confirm** | **for** |
| 1.910 MHz | adjust T1001 | Max S-meter |
| 3.7250 MHz | adjust T1002 | Max S-meter |
| 7.110 MHz | adjust T1004 | Max S-meter |
| 28.200 MHz | adjust T1012 | Max S-meter |

*IF Gain*

❒ Turn the transceiver off, then press and hold the **FAST** and **LOCK** buttons (near main VFO knob), and turn the transceiver on again.

❒ Connect the RF signal generator to the antenna jack, and inject +8 dBμ. Select menu function 9-1, and adjust the main VFO knob for a 1-segment S-meter deflection.

*S-meter full scale*

❒ Connect the RF signal generator to the antenna jack, and inject a +100 dBμ signal. Tune for peak indication on the S-meter. Adjust VR2002 for S9+60 dB on the S-meter.

*Noise Blanker*

❒ Preset the **NB** control fully clockwise, press the **NB1** switch on, and connect the DC voltmeter to TP2001. Inject +40 dBμ, and adjust T2001 and T2002 in succession several times for minimum DC voltmeter indication.

❒ Reduce the RF signal level to +20 dBμ, and confirm at least 3.2 V on the DC voltmeter. Select **NB2**, and also confirm at least 3.2 V.

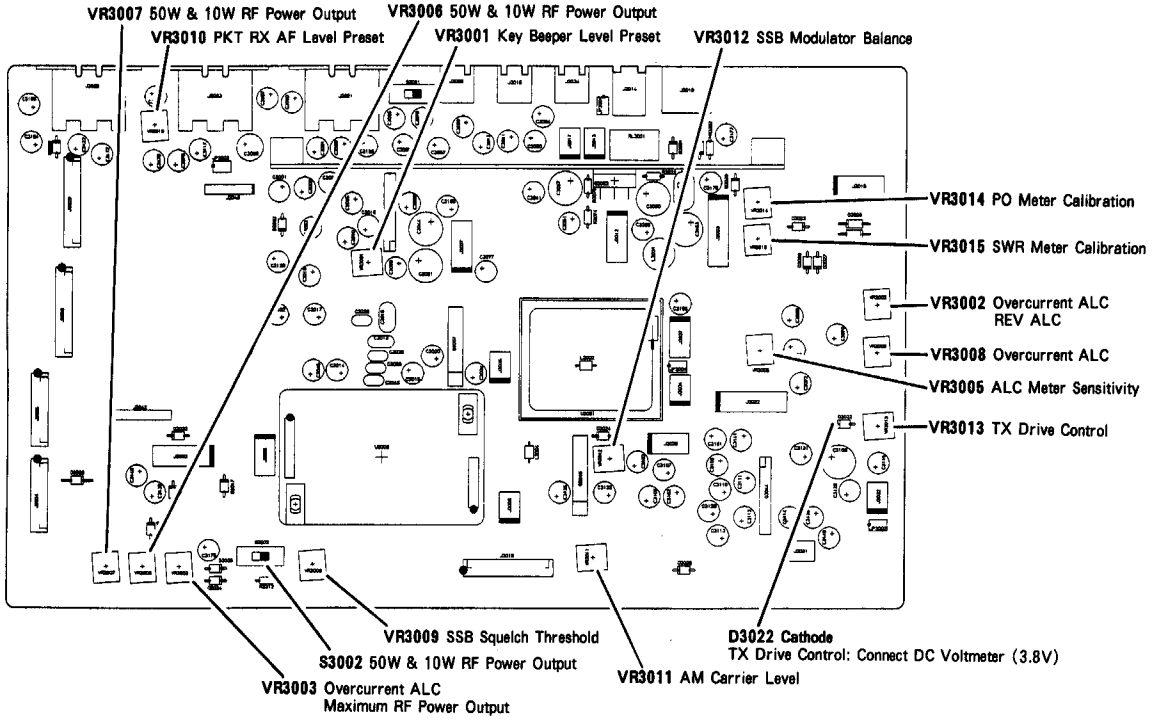
*IF NOTCH*

❒ Preset the **NOTCH** control for 12-o'clock, then inject a +40 dBμ signal at 14.2000 MHz to the antenna jack. Select USB, then tune the transceiver to 14.20150 MHz (so that a 1500 Hz tone is heard).

❒ Press the **NOTCH** button, then adjust VR2005 and L2004 for minimum S-meter indication.

*FM squelch threshold*

❒ With FM mode selected, and no signal present, set the **SQL** control to the 11-o'clock position, then adjust VR2001 so that the squelch just closes.




**AF Unit: Receiver Alignment Points**

*SSB squelch threshold*

❒ With USB selected, and no signal present, set the **SQL** control to the 10-o'clock position. Adjust VR3009 on the AF Unit so that the squelch just closes.

*Tx 2nd mixer*

❒ Select CW mode, and connect the spectrum analyzer to J2008. Key the transmitter, and adjust VR2006 to minimize the 2nd local spurious (±8.2 MHz from the 2nd local frequency).

*Transmitter IF interstage transformer*

❒ Connect the 50-Ω dummy load to the antenna jack. Preset the **RF PWR** control fully clockwise, and **MIC** gain control fully counter-clockwise. Select CW mode.

❒ Key the transmitter, and adjust T2013~T2015, T2017~T2019, T2021, T2023 in succession several times for maximum indication on the ALC meter.

*Overcurrent ALC*

❒ With the inline wattmeter and 50-Ω dummy load connected to the antenna jack, preset VR3002, VR3003, VR3008 on the AF Unit and the **RF PWR** control fully clockwise.

❒ Tune the transceiver to 3.500 MHz, and select CW mode. Key the transmitter and adjust VR3008 for 140 watts on the meter.

*Maximum RF power output*

❒ Preset the **RF PWR** control fully clockwise, and tune the transceiver to 14.2000 MHz. Select CW mode, the key the transmitter and adjust VR3003 for 100 watts on the meter.

*50W and 10W RF power output*

❒ Move switch S3002 from "100W" to the "50W" position. Connect the in-line wattmeter and 50-Ω dummy load to the antenna jack, select CW mode and tune to 14.2000 MHz.

❒ Set the **RF PWR** control fully clockwise. Key the transmitter, and adjust VR3007 for 50W on the power meter. Recall menu function 4-0, and select "10W".

❒ Key the transmitter, and adjust VR3006 for 10W on the power meter. After adjustment, recall menu function 4-0, then select "100W". Move switch S3002 back to the "100W" position.

*TX drive control*

❒ Set the **RF PWR** control fully counter-clockwise, and select CW mode. Key the transmitter, and adjust VR3013 for one segment displayed on the PO meter.

*ALC meter sensitivity*

❒ Set the meter function to ALC, then inject 4 mV at 1 kHz tone to the microphone jack. Key the transmitter, and adjust the **MIC** gain control so the meter just begins to deflect.

❒ Increase the injection level to 10 mV, and adjust VR3005 so that the meter deflects to the top edge of the ALC zone.

*TX IF gain*

❒ Turn the transceiver off. Next, press and hold **FAST** and **LOCK** (near MAIN VFO-A knob) button, then turn the transceiver on.

❒ For the frequencies listed in the table below, set the transceiver to LSB mode, and inject 0.5 mV at 1 kHz tone to the microphone jack. Set the **MIC** gain control fully clockwise.

**TX IF Gain Alignment**

Note: For all adjustments below, set the transceiver to LSB, and inject a 0.5 mV, 1-kHz to the MIC jack. Set the MIC GAIN control fully clockwise.

| Tune to: | Menu Function 92 | Key Tx and adjust MAIN VFO Dial for |
|---|---|---|
| 1.800 MHz | T IF-018 | Minimum ALC Indication |
| 3.500 MHz | T IF-035 | " " |
| 7.000 MHz | T IF-070 | " " |
| 10.000 MHz | T IF-100 | " " |
| 14.000 MHz | T IF-140 | " " |
| 18.000 MHz | T IF-180 | " " |
| 21.000 MHz | T IF-210 | " " |
| 24.500 MHz | T IF-245 | " " |
| 28.000 MHz | T IF-280 | " " |
| 29.000 MHz | T IF-290 | " " |

*PO meter calibration*

❒ With the wattmeter and 50-Ω dummy load connected to the antenna jack, select CW mode and set the meter to read power output.

❒ Key the transmitter, and adjust the **RF PWR** control for 100 W on the wattmeter. Then adjust VR3014 so the PO meter also indicates 100 watts.

*REV ALC*

❒ Connect the 16.6-Ω dummy load (or three 50-Ω loads in parallel), preset the **RF PWR** control fully-clockwise and select CW mode. Key the transmitter, and adjust VR3002 for 50 W on the PO meter.

# Alignment

*SWR Meter Calibration*

❒ Connect the 16.6-Ω dummy load (or three 50-Ω loads in parallel) to the antenna jack,then preset the **RF PWR** control fully-clockwise. Select CW mode and set the meter to read SWR.

❒ Key the transmitter, and adjust VR3015 so the meter indicates 3.0:1 SWR (within 1 bargraph segment).

*IC Meter Calibration*

❒ With the wattmeter and 50-Ω dummy load connected to the antenna jack, select CW mode and set the meter to read IC. Preset the **RF PWR** control fully-clockwise.

❒ Key the transmitter, and confirm 15A (± 3A) IC meter indication (within 1 bargraph segment).

*SSB Modulator Balance*

❒ With the 50 dB attenuator and spectrum analyzer (or 50-Ω dummy load and sampling coupler) connected to the antenna jack, and the **MIC** gain control preset fully counterclockwise, select CW mode. Alternatively, a separate receiver can be used, with the transceiver connected to the dummy load.

❒ Key the transmitter, and adjust VR3012 for minimum power output (carrier leakage, should be less than -50 dB) as indicated on the spectrum analyzer or external receiver.

*AM Carrier Level*

❒ With the wattmeter and 50-Ω dummy load connected to the antenna jack, select AM mode, set the meter to read ALC. With no microphone input, preset the **RF PWR** control to the fully clockwise. Key the transmitter, and adjust VR3011 for ALC meter deflects to the top edge of the ALC zone.

*Speech processor*

❒ Preset the T2016 to top edge of the coil case.

*COMP meter calibration*

❒ Set the **PROC** and **RF PWR** controls fully clockwise, and press the **PROC** button to activate the speech processor.

❒ Set the meter to read **COMP**, and preset the **MIC** gain control to the 1-o'clock position. Inject 2 mV audio at 1 kHz tone to the mic jack, and adjust VR2007 so that the transceiver's meter deflects to the 10 dB mark on the COMP scale.

*FM carrier frequency*

❒ Connect the frequency counter to J2008, preset the FM mic gain control fully counter-clockwise, and select FM mode. Key the transmitter, and adjust L2026 for 70.455 MHz ±50 Hz on the frequency counter.

*FM & CTCSS tone deviation*

❒ With the 50 dB attenuator and liner detector (or 50-Ω dummy load and sampling coupler) connected to the antenna jack, select FM mode, and tune to 29.2000 MHz .

❒ Set the FM mic gain control fully clockwise, and inject 10 mV at 1 kHz tone to the mic jack. Key the transmitter, and adjust VR2009 for ±2.3 kHz ±0.1kHz on the linear detector.

❒ Select the 88.5 Hz (default) subaudible tone, and press the **RPT** button to activate CTCSS operation. Key the transmitter and with no microphone input, and adjust VR2008 for 0.5 kHz ±0.1kHz on the liner detector.

*Transmitter carrier point*

❒ Turn the transmitter off, press and hold **FAST** and **LOCK** button (near main VFO knob), then turn the transceiver on.

❒ Recall menu function 9-0 and select "t-LSbcAr" using the SUB VFO-B dial.

❒ Select LSB mode and then inject a 1 kHz tone to the mic jack. Adjust the injection level to the point where the ALC meter no longer deflects.

❒ Adjust to inject frequency (within 800~2000 Hz) for peak RF output. Then adjust injection level for 80 W RF output.

❒ Set the injection frequency to 350 Hz, and adjust the MAIN VFO-A knob for 20 W RF output. Select "t-uSbcAr" using the SUB VFO-B knob, and select USB mode.

❒ Inject a 1-kHz tone to the mic jack, and adjust the injection level to the point where the ALC meter no longer deflects.

❒ Adjust the injection frequency (from 800 ~2000 Hz) for peak RF output, then adjust the injection level for 80 W RF output.

❒ Set the injection frequency to 350 Hz, and adjust the MAIN VFO-A knob for 20 W RF output.

*FM Mic Gain*

- ❒ With the 50 dB attenuator and linear detector (or 50-Ω dummy load and sampling coupler) connected to the antenna jack, tune to 29.200 MHz, and select FM mode.
- ❒ Inject a 1.5 mV signal at 1 kHz to the mic jack. Key the transmitter, and adjust VR6807 for 1.75 kHz ±0.1 kHz on the linear detector.

*PKT Receiver AF Level Preset*

- ❒ Preset VR3010 fully clockwise.

*Key beeper level preset*

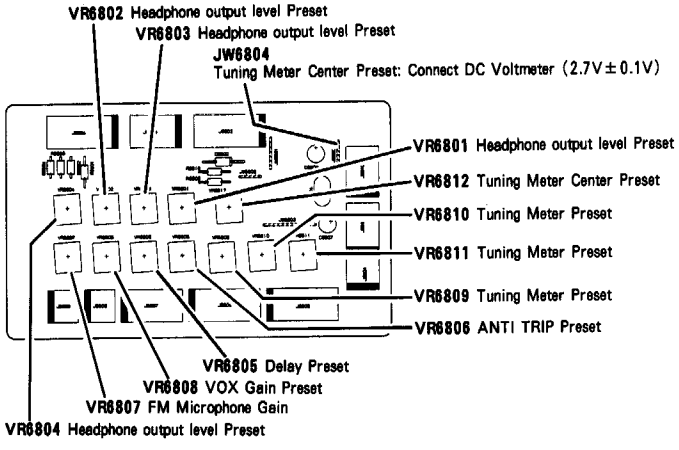
- ❒ Preset VR3001 fully counter-clockwise.

*Headphone Output Level Preset*

- ❒ Preset VR6801, VR6802, VR6803 and VR6804 to their 12-o'clock positions.

*Tuning Meter Center Preset*

- ❒ Preset VR6809~VR6812 to their 12 o'clock positions. Select CW mode, and turn the **SPOT** function on.
- ❒ Connect the DC voltmeter to JW6803, and adjust the **PITCH** control for at least 4.0 V on the DC voltmeter.
- ❒ Connect the DC voltmeter to JW6804, and adjust VR6811 for 2.7 V ±0.1 V on the DC voltmeter.
- ❒ Adjust VR6812 for a centered tuning meter indication.




**ALC Unit: Test & Alignment Points**

*Tuning Meter Preset (CW, RTTY and PKT mode)*

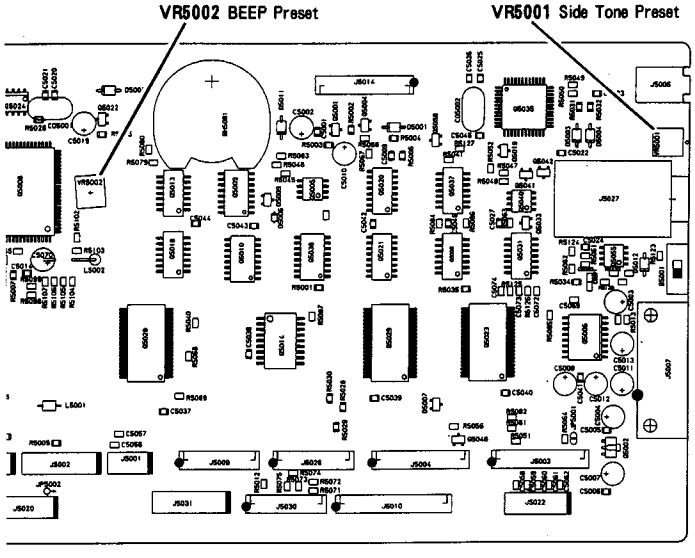
- ❒ Recall menu function 3-5 and select "A1-PitcH" using the MAIN VFO-A knob. Tune to 700 Hz using the **PITCH** knob ("C-700" displayed).
- ❒ Select CW mode, press the **SPOT** key, and adjust VR6811 for a centered tuning meter indication.
- ❒ Select menu function 4-2, select RTTY mode, and tune to 2210 Hz using the MAIN VFO-A knob.
- ❒ Select "bEEP-tun" using the SUB VFO-B knob, and adjust VR6810 for a centered tuning meter indication.
- ❒ Tune a 2125 Hz beep frequency using the MAIN VFO-A knob, and select **PKT** mode. Select "bEEP-tun" using the SUB VFO-B knob, and adjust VR6809 for a centered tuning meter indication.

*VOX gain, ANTI TRIP and delay preset*

- ❒ Preset VR6805 (DLY), VR6806 (ANTI TRIP) and VR6808 (VOX gain) to their 12-o'clock positions.

*BEEP and SIDETONE Preset*

- ❒ Preset VR5001 (SIDETONE) and VR5002 (BEEP) to their 10-o'clock positions.




**CNTL Unit: Test & Alignment Points**

Notes:

## *Main Receive Signal Circuitry*

### *High-Frequency Circuit*

The receive signal, input from ANT connector A or B and selected by relays RL8701/RL8702 on the ANT Unit, passes through connector J8702, the HPF unit, and t/r relay RL6016 on the LPF Unit and is led to connector J1001 on the RF Unit from connector J6006.

The receive signal then passes through receive antenna switching relay RL1001 and an attenuator (-6 dB, -12 dB) which consists of resistors R1039, R1040, R1051, and R1064 and relays RL1002 and RL1003. It then enters a 5th-order Chebyshev low-pass filter (LPF) which consists of coils L1039 and L1040 and capacitors C1081, C1082, C1091, C1092, and C1093. After the signal is removed of frequency components of 30 MHz and over, it is led to a band-pass filter (BPF).

This BPF is a 5th-degree apolar Chebyshev type filter which divides the frequency range 100 kHz to 30 MHz into 11 bands. According to the receiving frequency, the appropriate band is selected by diodes D1003, D1004, D1007-D1010, D1015-D1019, D1025, D1026, D1029, D1030, D1035, D1036, D1039, D1040, D1044-D1049, D1053, D1054, D1056, and D1057. After the signal is removed of unwanted frequency components, it is applied to the high-frequency amplifier circuit.

The RF amplifier consists of low-band amplifier circuit FET Q1004, mid-band amplifier circuit FET Q1009, Q1011, Q1013, and Q1014, and high-band amplifier circuit Q1020. The appropriate amplifier circuit is selected* by D1005, D1006, D1013, D1014, D1023, D1032, D1037, D1041, and D1043. After amplification, the signal passes is applied to the 1st mixer circuit and sub-receive circuit (RX2 Unit).

***Note*** - if FLAt is selected in Menu Program 8-4, RF signal input is input to the mid-band amplifier circuit.

Diodes D1001 and D1002, which are connected to the RF amplifier input and output, turn on (off) the amplifier circuit via the front-panel IPO switch.

### *1st Mixer Circuit/1st IF Circuit*

The 1st mixer of the RF Unit consists of FET Q1027, Q1028, Q1030, and Q1031. The 1st local signal (70.555 ~ 100.455 MHz) from the LOCAL Unit is amplified by Q1021 and applied to each FET gate of the 1st mixer.

The resulting output signal (the difference between the local signal and receive signal) passes through dual monolithic crystal filter (MCF) XF1001/1002 (BW: ±6 kHz) to obtain the 1st IF signal having a center frequency of 70.455 MHz. The signal is fed to the 2nd mixer circuit of the IF Unit after it is amplified by FET Q1029.

### *2nd Mixer Circuit/2nd IF Circuit*

The 2nd mixer consists of FET Q2020 and Q2024 of the IF Unit. The 2nd local signal (62.24 MHz) from the LOCAL Unit is amplified by Q2027 and applied to each FET gate of the 2nd mixer.

The output from the 2nd mixer passes through monolithic crystal filter (MCF) XF2001, where it is stripped of unwanted signal components to become the 2nd IF signal (8.215 MHz). A portion of the 2nd IF signal from the mixer output is fed to the FM IF circuit through a noise blanker circuit and buffer-amplifier FET Q2003.

The 2nd IF signal that has passed through the MCF enters the noise blanker gate (NB Gate) which consists of D2014. It is then routed through either a crystal filter (XF2002, XF2003, U2002, U2005) or an attenuator (R2174, R2175, R2183), according to receiving mode (CW, SSB, or AM), to the 3rd mixer circuit after it is buffer-amplified by FET Q2052.

### *Noise Blanker Circuit*

The signal sampled from the 2nd IF circuit is amplified by FET Q2009 and Q2010 on the IF Unit and then undergoes detection by D2006. This output passes through R2017 and R2027, C2006, and Q2001 to become an average AGC voltage for controlling the degree of amplification of the above FETs. Noise pulses contained in the output from D2026 are detected by Q2009 and Q2013 and used to control the NB Gate.

*3rd Mixer Circuit/3rd IF Circuit (IF Notch Circuit)*

The 3rd mixer uses double-balanced mixer IC Q2021 (DBM) on the IF Unit. The 3rd local signal (8.67 MHz) from the LOCAL Unit is input to the DBM IC local port after it is buffer-amplified by Q2028. The signal output from the 3rd mixer passes through a ceramic filter, crystal filter, or mechanical filter (U2001, U2003, U2004, U2006, CF2002), to become the 455-kHz 3rd IF signal.

The 3rd IF signal that is buffer-amplified by Q2025 passes through a notch frequency control circuit which consists of L2004, C2063, C2064, and D2020. Attenuation in the IF notch circuit is controlled by VR2005. Th 3rd IF is then buffer-amplified by Q2023 and further amplified in two stages by FET Q2026 and Q2029.

The IF signal is then buffer-amplified by Q2004 and Q2017, respectively. The output of Q2004 is applied to the AF Unit through connector J2002, and the output from Q2017 is input to the AGC circuit.

*AGC Circuit*

The AGC circuit consists of D2012 and D2013, transistor Q2018, etc. on the IF Unit. Output from the AGC circuit is input to the RF AGC circuit that consists of FET and PIN diodes of the IF amplifier stages, by which the output is controlled.

*FM IF Circuit/FM Demodulator Circuit*

The 2nd IF signal that has passed through buffer-amplifier FET Q2003 on the IF Unit, and the 3rd local signal (8.67 MHz) that has been buffer-amplified by Q2028 are input to IC Q2015 for FM demodulation.

The FM demodulator IC contains a mixer, limiter amplifier, filter amplifier, squelch trigger, and demodulator. The IF input signal is mixed with the 3rd local signal, band-limited by ceramic filter CF2001 (BW: ±4 kHz), amplified by the limiter amplifier, and demodulated into an audio signal by the demodulator. It then passes through a filter (R2028, C2021) and connector J2004 and input to the AF Unit. The signal then enters analog switch IC Q3001-3 through a de-emphasis circuit which consists of R3060 and C3052.

The squelch circuit selectively amplifies the noise component of the demodulator output by the filter amplifier inside the FM IC and the active band-pass filter consisting of an externally attached resistor and capacitor. This circuit uses a signal detected by D2001.

*SSB/CW Demodulator Circuit*

The 3rd IF signal from the IF Unit is applied to the SSB demodulator (SSB DET) of Q3007 on the AF Unit, which produces audio by applying the carrier signal from the DDS-CAR Unit to Q3007 after buffer-amplifying it by Q3020. Similarly, the CW signal is demodulated by a carrier signal which is offset by the pitch frequency.

The demodulated SSB and CW signals are each stripped of high-frequency components by an active low-pass filter consisting of op-amp IC Q3008-2 and IC Q3008-1. Then, they enter analog switch IC Q3001-2 and IC Q3001-4.

*AM Demodulator Circuit*

The 3rd IF signal from the IF Unit is input to I-DET Unit U3003 on the AF Unit, from which it enters IC Q3703 for AM demodulation.

The IC for AM demodulation consists mainly of an envelope detector, VCO, phase shifter, synchronous detector, and DC/AC detector. From the IF signal that is input to the IC, the envelope detector output and synchronous detector output are picked up.

The output from the demodulator circuit passes through analog switch Q3701-1 and Q3701-2 for switching between the synchronous detector output and envelope detector output. It then enters analog switch IC Q3001-1 after removed of the high-frequency components by an active low-pass filter (op-amp IC Q3013-1) on the AF Unit.

*Low-Frequency Amplifier Circuit*

The demodulated signal that is selected by one of analog switches IC Q3001-1 to IC Q3001-4 on the AF Unit according to receiving mode passes through the squelch switch, audio muting FET Q3002, low-frequency amplifier transistor Q3006, electronic volume IC Q3005, op-amp IC Q3014-1 for buffer-amplification, and IC Q3022 for low-frequency power to drive the internal or external speaker with a maximum output of approximately 1.5 W. The signal that passes through electronic volume IC Q3005 is also output to the headphone terminal after it is amplified by headphone amplifier IC Q3015-1.

## *Transmit Signal Circuitry*

### *Microphone Amplifier Circuit*

The audio signal from microphone jack J9421 on the MIC Unit is passed through board-in connector JP9421 and DISPLAY Unit's connectors (J5528 and J5529), amplified by transistor Q3048 on the AF Unit, and input to electronic volume IC Q3044 which is controlled by the MIC knob on the panel.

The output (audio signal) from the electronic volume is amplified by Q3045 and input to modulator circuit IC Q3046 through the buffer-amplifier transisitor (Q3043). During FM reception, the audio signal is input to connector J2011 inside the IF Unit after its volume is adjusted by VR6807 on the ALC Unit.

The audio signal that has passed through the pre-emphasis circuit consisting of C2201 and R2228 on the IF Unit is mixed with a tone signal from the CNTL Unit and amplified and limited by op-amp IC Q2049-2 of the IDC circuit. The audio then passes through the splatter filter (secondary active low-pass filter) formed by op-amplifier IC Q2049-1, R2229 and R2230, and C2119 and C2206 is then input to the frequency-modulator circuit inside the IF Unit through VR2008 and VR2009 for setting frequency deviation.

### *SSB Modulator Circuit*

The carrier signal appropriate to the transmitting mode (LSB, USB) is applied from the CAR-DDS Unit to balanced modulator (BM) IC Q3046 of the AF Unit and modulated by microphone audio.

The balanced modulator outputs the upper and lower side bands and carrier signal. The carrier and audio signal are suppressed and the carrier balance is adjusted by VR3012. As a result, the output signal obtained is a DSB signal with a carrier suppression ratio of 35 dB or more.

The side-band modulated signal (1st IF signal: 455 kHz) from the BM IC is input to mechanical filter XF9801 inside the SSB-FIL Unit on the IF Unit through buffer-amplifier Q3049, connector J3026, and IF Unit's connector J2009.

The DSB signal picks up the required side-band modulated signal by mechanical filter XF9801 inside the SSB-FIL Unit and applies it as an SSB signal to the transmission frequency mixer at the next stage.

### *AM Modulator Circuit*

As in the SSB modulator circuit, a carrier signal appropriate to the transmitting mode (AM) from the CAR-DDS Unit and an audio signal from the microphone are input to balanced modulator (BM) IC Q3046 of the AF Unit.

The control signal from CPU IC Q5008 in the CNTL Unit causes a voltage of AM 9 V to be output from transistor array IC Q5025. This voltage is applied via VR3011 and D3018 to IC Q3046, causing the balanced modulator to lose balance. The carrier signal and modulated signal are then input to the Tx mixer via ceramic filter CF2002 inside the IF Unit.

### *Frequency Modulation Circuit*

The FM circuit uses a voltage controlled crystal oscillator (VCXO) consisting mainly of IF Unit oscillator Q2044, X2001, varactor D2049, and L2026. The VCXO has a center frequency of 8.215 MHz.

The FM signal is produced by applying a signal from the FM microphone amplifier circuit to varactor D2049 and varying the crystal oscillator load capacity in proportion to the signal voltage. The FM signal is input to gate 1 of 2nd IF circuit FET Q2036 via Q2043 for buffer amplification and D2034.

### *CW (A1) Signal Generator Circuit*

When the transmitting mode is CW (A1), the control signal from CPU IC Q5008 in the CNTL Unit causes a CW 9 V voltage to be output from transistor array IC Q5025. While microphone audio is cut off by Q3050, the voltage is applied to balanced modulator IC Q3046 via D3018, providing a carrier from the balanced modulator for input to the transmit signal circuit of the IF Unit.

### *1st IF Circuit/1st Mixer Circuit*

The 455 kHz 1st IF signal from the modulator circuit is band-limited by the IF Unit's ceramic or mechanical filter CF2002, U2001 (XF9801) according to the selected mode (CW, SSB, or AM). It is then buffer-amplified by FET Q2037 and input to 1st mixer circuit IC2030.

As the 1st mixer, the IF Unit's double balanced mixer IC Q2030 (DBM) is used. A local signal (8.67 MHz) from the LOCAL Unit which is buffer-amplified by transistor Q2028 and input to the local port

of DBM IC is mixed with the 455 kHz 1st IF signal to produce a 8.215 MHz 2nd IF signal.

*2nd IF Circuit/2nd Mixer Circuit*

The 2nd IF signal passes through either the IF Unit's crystal filter (XF2002, XF2003, U2002, U2005) or attenuator (R2174, R2175, R2183), whichever is appropriate to the selected mode (CW, BBS, or AM). It is then amplified by FET Q2036 and input to the 2nd mixer circuit.

The 2nd mixer consists of the IF Unit's FET Q2033 and Q2038. A 2nd local signal (62.24 MHz) from the LOCAL Unit is amplified by Q2027 and input to each FET gate. The signal that is output from the 2nd mixer is removed of unwanted signal components as it passes through a filter formed by T2014/T2017 and C2227 to obtain a 70.455 MHz 3rd IF signal.

*3rd IF Circuit/3rd Mixer Circuit*

The 3rd IF signal passes through T1023, is amplified by FET Q1034, then input to the 3rd mixer circuit via T1021. There it mixes with a local signal (72.255 ~100.455 MHz) generated by the LOCAL Unit to produce a transmit signal (1.8 MHz to 30 MHz) is generated.

*High-Frequency Amplifier Circuit (Transmit Preamp. Circuit)*

The transmit signal is passed through a low-pass filter which consisting of L1086/L1087 and C1208/C1209/C1212/C1213/C1214, wide-band amplified by Q1024, and input to the PA Unit via Q1022/Q1023 for buffer amplification and exits via connector J1007.

*Power Amplifier Circuit*

A transmit signal from the RF Unit is input to connector J6101 of the 100W-PA Unit .

The transmit signal (1.8 MHz to 30 MHz) input to the 100W-PA Unit is amplified by Q6101-Q6105 (pre-driver, driver, and final) and output from connector J6102 to the LPF Unit.

*Low-Pass Filter Circuit*

The transmit signal from the power amplifier circuit is input to connector J6001 of the LPF Unit and passed through an LPF consisting mainly of RL6001-RL6014, L6001-L6014, and various capacitors. The LPF is a 5th-degree simultaneous Chebyshev type filter which divides the transmission frequency range (1.8 MHz to 30 MHz) into seven bands.

The low-pass filtered transmit signal is input to the ANT Unit through CM coupler L6015, tuner switching relay RL6015, ANT relay RL6016, and connector J6005.

The CM coupler, which consists mainly of L6015, TC6001, and C6056, samples a part of the transmission power to detect traveling-wave power and reflected-wave power. A detected voltage is produced by D6002-D6005, and is used for automatic level control (ALC).

*ALC Circuit*

The output from the CM coupler is, as the detected traveling-wave (FWD) and reflected-wave (REV) voltage, routed from connector JP6002 through connectors J6810/J6811 in the ALC Unit and applied to the ALC circuit via connector J3018 in the AF Unit.

The ALC circuit consists of an op-amplifier circuit for amplifying traveling-wave and reflected-wave voltage, time-constant ALC amplifier, and transmit signal control circuit in the IF Unit.

The traveling-wave voltage (FWD) from connector J3018 in the AF Unit is added with a DC control voltage which passes through the output power control, VR3003 (for setting transmission output, etc., on the panel(, and is then applied to op-amplifier IC Q3026-1.

The detected reflected-wave voltage (REV) is added with a DC control voltage which passes through VR3088, and is then applied to op-amplifier IC Q3026-2. In high SWR conditions (SWR 1:3 or more), transmitter output is reduced and warning appears, thus, the PA Unit is protected.

The op-amp output passes through D3009 where the forward and reflected output from the op-amplifier are mixed and input to the ALC amplifier, which contains a time-constant circuit.

The ALC amplifier sufficiently amplifies the forward and reflected-wave output via transistor Q3025. This output then passes through a fast-attack, slow-delay RC time-constant circuit consisting of R3083/R3087 and C3069/C3157 for input to the Tx signal control circuit via connector J3015 and J2004 on the IF Unit.

The TX control circuit adjust the IF amplifier gain via gate 2 of FET Q2036 of the 8.215 MHz IF amplifier circuit to prevent the Tx output from exceeding the preset level.

*Keying Circuit*

When electronic keyer is used in CW mode, the bias of Q1024 and 2nd/3rd mixer FET Q2033/Q2038/Q1034 is controlled via NAND gate IC Q1026 and Q1019 to generate CW.

To limit modulation, keyer input is optimized by time-constant circuits, such as D1042, R1077, and C1129 of the bias control circuit, to limit bandwidth.

*PLL Frequency Synthesizer (Main)*

The PLL Frequency Synthesizer consists mainly of a master reference oscillator circuit, 2nd local oscillator circuit, 3rd local oscillator circuit, DDS-PLL/DDS-SUB/DDS-CAR units which digitally synthesize carrier outputs, and a PLL circuit which contains a voltage controlled oscillator (VCO).

*Master Reference Oscillator Circuit*

The master reference oscillator uses a Colpitts circuit (oscillation frequency: 10.48576 MHz) composed of Q4701, X4701, TC4701, and C4709/C4711. The reference oscillator signal passes through a low-pass filter composed of buffer amplifier Q4702, C4712/C4713, and L4701. It is then input to the LOCAL Unit via J4702, and also to the RX2, AF, and DSP-D Unit as the reference oscillation frequency.

*DDS-CAR Unit/DDS-PLL Unit/DDS-SUB Unit*

DDS IC Q3601/Q4502/Q4603 of the DDS (Direct Digital Synthesizer) Units each contain a shift register, selector, phase accumulator, and ROM.

The reference oscillation frequency (10.48576 MHz) that is input to each of the DDS Units is applied to DDS IC after amplified by transistors Q3603/Q4503/Q4601.

DDS outputs contain digital amplitude data corresponding to serial frequency data from CPU IC Q5008 of the CNTL Unit. The digital amplitude data is D/A-converted by ladder resistors RB3601/RB4501/RB4601 and passes through buffer amplifier Q3602/Q4501/Q4602 and Chebychev LPF to generate a sine wave. The DDS frequency range is 453.5 ~ 466.74 kHz (cf = 455.0 kHz) for CAR-DDS, 373.08 ~ 291.16 kHz for DDS-PLL, and 907.88 kHz ±620 Hz for DDS-SUB.

*3rd Local Oscillator Circuit*

The 3rd L.O. circuit generates a 1.81576 MHz signal by doubling the 907.88 kHz output from the SUB-DDS Unit on the LOCAL Unit by a filter composed of Q4039, T4010, C4153/C4164/C4170, and L4038. The doubled signal is input to mixer Q4027.

At the mixer, the 1.8-1576 MHz input signal is mixed with the 10.48576 MHz reference oscillation signal. The mixer output is stripped of unwanted frequency components by T4009 and monolithic filter XF4001 to generate the 8.67 MHz 3rd L.O. signal.

This signal is amplified by Q4029 and T4008 and passes through buffer amplifier Q4017 and a LPF composed of C4098/C4099/C4172 and L4022 for input to the IF Unit via connector J4003.

*2nd Local Oscillator Circuit*

The 2nd L.O. circuit is a Hartley-type overtone oscillator circuit (frequency: 62.24 MHz) composed of FET Q4003 T4001, and X4001 in the LOCAL Unit. It then passes through amplifier Q4012, T4006/T4007, and C4043, for input to the IF Unit via connector J4002.

*1st Local Oscillator Circuit*

VCO output is buffer-amplified by Q4004/Q4005 and passes through a LPF composed of L4003/L4004 and C4028, C4029, C4033-C4035. It is then input to the Tx/Rx frequency mixer circuit of the RF Unit via connector J4001.

*PLL Circuit*

The PLL circuit is a frequency mixing type composed of a VCO, mixer, PLL IC, and loop filter.

The VCO consists of four circuits—VCO1, VCO2, VCO3, and VCO4, with a frequency range of 70.555 ~ 100.455 MHz divided into four bands, allocated to the four VCO circuits. The range of VCO1 is further divided by a circuit which shifts the oscillation frequency. VCO1-VCO4 consist mainly of FET Q4009/Q4016/Q4023/Q4032, D4001/4002/4004/4005/4007/4008/4010/4011, TC4001-TC4004, and L4013/4020/4029/4035.

The VCO switching signal from connector J4004 is used to drive switching transistors

Q4013/4021/4026/4037 to switch the source terminal of the oscillator FET.

VCO1 uses the VCO0 control signal to drive switching transistors Q4039/Q4040, apply a forward bias to D4013, and switch C4173 into the oscillator circuit, producing a frequency shift.

The 70.555~100.455 MHz VCO signal is input to mixer Q4001 via buffer amplifier FET Q4007 and buffer amplifier Q4006.

The 3rd local signal (8.67 MHz) that has been buffer-amplified by Q4022 and passed through the LPF composed of C4112/4113/4118-4120 and L4026/4027, the reference oscillator signal (10.48576 MHz) from the REF Unit that has been amplified by transistor Q4025, divided into 2.62144 MHz by 1/4-frequency divider Q4020, and passed through a low-pass filter composed of C4105/4106/4108-4110 and L4024/4025 are input to mixer Q4019 to obtain a 6.04856 MHz signal.

This 6.04856 MHz signal is stripped of unwanted signal components by ceramic filter CF4002 and input to mixer Q4010, together with the 291.16-373.08 kHz output frequency of the DDS-PLL Unit, to obtain a 5.67548~5.75740 MHz signal. This signal passes through CF4001 to mixer Q4002, together with the 62.24 MHz 2nd L.O. output that has been buffer-amplified by Q4011, to obtain a 67.91548~67.99740 MHz signal.

This signal passes through a BPF composed of T4003-T4005 and C4011/4012, buffer-amplified by Q4008, and input to mixer Q4001 via transformer T4002.

The mixer output from Q4001 (2.62144~32.52224 MHz) passes through a 9th-degree simultaneous Chebychev LPF composed of L4007-L4011 and C4048-C4052, C4061-C4066 is amplified by FET and Q4015/4018 and input to PLL IC Q4024.

At the same time, the 10.48576 MHz reference oscillator signal from the REF Unit is input to PLL IC Q4024 after it is amplified by Q4030 and passes through buffer amplifier Q4028 and a LPF composed of C4148/C4149 and L4033.

The phase is compared between the reference frequency and the frequency of the signal input to PLL IC, and a signal whose pulse corresponds to the phase difference is produced. The VCO frequency is controlled by a loop filter which consists of an active filter composed of Q4033, Q4034/Q4038, R4089/R4091, and C4153 and a secondary lag filter composed of R4088 and C4059 / 4095 / 4128 / 4160 /4158.

*Carrier Oscillation Signal Circuit*

The 453.5~466.74 kHz (cf = 455.0 kHz) carrier output from the DDS-CAR Unit passes through buffer amplifier Q3020 and a LPF composed of L3002 and C3063/C3064. The signal path is switched by D3003/D3005 during Tx/Rx so that the signal is input to balanced modulator IC Q3046 and SSB detector Q3007.

## *RX2 Circuit*

*Receive Signal Flow*

A portion of the receive signal from the RF Unit is input to J8002 of the RX2 Unit via J1003. It then passes through T8008 and input to 1st mixer Q8022/Q8027. The 47.31~77.21 MHz 1st L.O. signal output from the RX2 PLL circuit is input to the 1st mixer. The resulting 47.21 MHz 1st IF signal then passes through monolithic filter XF8001 (band width: ±20 kHz), amplified by Q8024, and input to the 2nd mixer circuit.

The 46.755 MHz 2nd L.O. and the 1st IF signal are mixed in Q8023/Q8026 to generate a 455 kHz 2nd IF signal. This signal is then input to noise-blanker noise amplifier Q8008, noise gates (D8010/D8028), and FM signal buffer amplifier Q8001, respectively.

The 2nd IF signal, now removed of noise by the noise gates, is passed through either CF8002/CF8003 or U8001 to become the desired signal component. It is then amplified by FET Q8048 and Q8049 and input to the SSB demodulator circuit through a buffer amplifier.

The 2nd IF signal that has been input to the SSB demodulator circuit is input to IC Q8057, together with a carrier signal from the RX2 CAR-DDS Unit, and demodulated into an audio signal.

The demodulated audio signal is removed of wide-band frequency components as it passes through buffer amplifier transistor Q8017 and active LPF Q8013. It is then input to analog switch Q8006.

The signal that has passed through the buffer amplifier is passed on to the AM detector circuit and

AGC circuit. An AM signal detected by D8014 is input to analog switch Q8006.

The audio signal that has passed through analog switch Q8006 then passes through mute switch FET Q8002, and is amplified by Q8015, before input to the electronic volume of the AF Unit via connector J8001.

*AGC Circuit Operation*

The receive signal that has passed through buffer amplifier Q8029 is rectified by AGC detector D8017/8018 to control gate 2 of FET Q8024/Q8048 by transistor Q8021. This signal is also amplified by op-amplifier Q8005/Q8011 for S-meter and squelch control.

*RX2 PLL Frequency Synthesizer*

The 2nd L.O. circuit is a Hartley-type overtone oscillator circuit (frequency: 46.755 MHz) composed of FET Q8046 and crystal X8001 in the RX2 Unit and transformer T8018.

The oscillation signal from this circuit is input to the 2nd mixer via Q8044 and T8017/T8016. Like the main PLL circuit, the PLL circuit is a frequency mixing type composed mainly of a VCO, mixer, PLL IC, and loop filter.

The VCO consists of four circuits—VCO1 through VCO4. The 47.31~77.21 MHz oscillation frequency range is divided into four bands, which are allocated to the four VCO circuits.

VCO1 to VCO4 are composed of oscillator FET Q8034/8047/8051/8058, variable-capacity diodes D8021/8024/8027/8031, and oscillator coils L8007/8010/8020/8024. The VCO switching signal from connector J8003 drives switch transistors Q8040/8050/8056/8063 to switch the source line of each oscillator FET.

The oscillation signal (47.31 ~ 77.21 MHz) from VCO is input to mixer Q8043 through buffer amplifier FET Q8041 and buffer amplifier transistor Q8042.

The reference oscillator signal (10.48576 MHz) from the LOCAL Unit that has been amplified by Q8066/Q8060 and divided into 5.24288 MHz signals by Q8054 is input to mixer Q8055 through a LPF composed of C8152/8153/8164/8165/8166 and L8012/L8013.

At the same time, the 286.28~364.20 kHz output from the RX2 PLL-DDS Unit is input to mixer Q8055 to obtain a 5.52516~5.60708 MHz signal.

This signal passes through ceramic filter CF8004 and is input to mixer Q8038, together with the 46.755 MHz output of the 2nd L.O. that has been buffer-amplified by Q8045 to produce a 41.14792~41.22984 MHz signal. This is then passed through a BPF composed of T8013/T8014 and C8087, amplified by Q8037, and then input to mixer Q8043 via T8012.

The output of mixer Q8043 ranges from 6.1440 ~ 36.0488 MHz, and passes through a 9th-degree simultaneous Chebyshev LPF which is composed of L8015-L8019 and C8157-1861/C8168-8173. This is input to PLL IC Q8061 after it is amplified by FET Q8053 and transistor Q8052.

At the same time, the 10.48576 MHz reference oscillatior signal from the LOCAL Unit is also input to PLL IC Q8061 via buffer amplifier Q8064 after amplification by Q8065.

The phase is compared between the reference frequency and the frequency of the signal input to the PLL IC, and a pulse corresponding to the phase difference is output to control the VCO frequency by a loop filter consisting of an active filter composed of FET Q8059, transistor Q8062, resistor, and capacitor and a secondary lag filter composed of a resistor and capacitor.

The controlled VCO output is amplified by Q8035/Q8036 and passed through a LPF composed of L8005/L8006 and C8098/C8099/C8104-8106. It is then input to the 1st mixer circuit through an attenuator.

*DSP Circuit*

The DSP circuit consists mainly of DSP (Digital Signal Processor) IC Q7101, AD/DA converter IC, and filter circuit. The functions performed by this circuit are SSB, AM demodulation, auto-notch, noise reducing, audio filtering, etc. in the receiving system and SSB generation/modulation and audio equalizing in the transmission system.

*Analog-Digital Converter Circuit (Transmission System)*

The audio signal from the microphone that has passed through electronic volume Q3044 in the AF Unit is input to the DSP-A Unit through connectors

J3037/J7001. It then passes through a 5th-degree active HPF (cut-off frequency fc = 80 Hz) composed of op-amplifier IC Q7004-1/Q7004-2, R7001-7004/R7007, and C7001/C7002/C7004-7006 to eliminate unwanted frequency components below the cut-off frequency.

The signal then passes through a inverting/non-inverting buffer amplifier circuit composed of op-amplifier IC Q7005-2 to Q7005-4 and input to A/D converter IC Q7001, where it is converted into a 16-bit digital signal. As 16-bit serial data, this signal is transmitted to DSP IC Q7101 in the DSP-D Unit via connector J7003.

*Digital-Analog Converter Circuit (Transmission System)*

The serial digital data input to the D/A converter IC Q7001 is converted into an analog signal and passed through a differential amplification type tertiary LPF (cut-off frequency fc = 18 kHz) composed of op-amplifier IC Q7007-1/Q7007-2, R7037-R7043, and C7043-C7046 to suppress out-of-band, random noise, etc. The signal is then input to the AF Unit as an audio signal or SSB signal of 10.24 kHz suppressed carrier via connector J7001.

*Digital Signal Processor Circuit (Transmission System)*

In the transmission system, this circuit has a microphone equalizing function and digital modulator function. The A/D-converted signal data is subjected to tone quality processing and input to a digital modulator. When desired, it is possible to disable microphone equalizing and digital modulation. The serial audio data or SSB (LSB or USB) data processed by DSP IC is input to the D/A converter in the DSP-A Unit via connector J7103.

The signal from the DSP Unit is input to balanced modulator IC Q3046. When the DSP-enabled SSB modulation function is used, the balanced modulator IC operates as a double balanced mixer (frequency mixer). In this case, a carrier (local) signal (LSB = 466.74 kHz, USB = 463.74 kHz) generated by the DDS-CAR Unit and SSB signal of 10.24 kHz suppressed carrier apply a mixed output of 455 kHz differential frequency to ceramic filter CF2002 via connector J2009 in the IF Unit. Thus, this circuit performs the same operations as the analog circuit.

When only the equalizing function is used in A3 mode, the circuit operations after balanced modulator IC Q3046 are the same as those of the analog circuit.

*Analog-Digital Converter Circuit (Receiving System)*

The audio signal passing through balanced modulator IC Q3007 in the AF Unit or SSB signal of 10.24 kHz suppressed carrier is input to the DSP-A Unit via connectors J3037/J7001. It then passes through a inverting/non-inverting buffer amplifier circuit composed of op-amplifier IC Q7006-2 then to Q7006-4 and finally input to A/D converter IC Q7001, where it is converted into a 16-bit digital signal. As 16-bit serial data, this signal is input to DSP IC Q7101 in the DSP-D Unit via connector J7003.

*Digital-Analog Converter Circuit (Receiving System)*

The serial digital data that is input to D/A converter IC Q7001 is converted into analog data and passed through a differential amplification type tertiary LPF (cut-off frequency fc = 18 kHz) composed of op-amplifier IC Q7008-1/Q7008-2), R7037-R7043, and C7043-C7046 to suppress out-of-band quantigation noise, etc. It is then input to the AF Unit as an audio signal via connector J7001.

*Digital Signal Processor Circuit (Receiving System)*

During receive, this circuit performs audio processing and SSB/CW/AM demodulation. The A/D-converted signal data is subjected to digital demodulation and audio processing. When appropriate, it is possible to disable the digital demodulation and audio processing.

When the DSP demodulation function is used, balanced mixer IC Q3007 of the AF Unit operates as a double balanced mixer (frequency mixer). In this case, the 3rd IF signal (455 kHz) from the IF Unit is mixed with a carrier (local) signal of the frequency ($f_{LSB}$ = 466.74 kHz, $f_{USB}$ = 463.74 kHz) generated by the DDS-CAR Unit to produce a differential frequency of 10.24 kHz. The audio data processed by DSP IC is serially input to the D/A converter in the DSP-A Unit.

## Control Circuitry

### Microprocessor Circuit

The microprocessor circuit, which is composed of CPU IC Q5008 and EEPROM IC Q5024, performs various types of processing, such as the control of various control signals, serial I/O, A/D converter, dial counter circuit, key input, and display.

The EEPROM memorizes various parameters and settings (transmission frequency range, transmission output control) and carrier points according to transceiver version and the contents of memory channels.

### Reset Circuit

The reset circuit consists mainly of CNTL Unit IC Q5005/5022/5039-5, capacitors, and resistors. This circuit controls the power-down input port, CPU reset input, keyer CPU, and related circuits.

### Dial Counter Circuit

The dial counter circuit consists of two VFO dials, MEM dial, CLAR dial, and IC Q5026/Q5027. This circuit detects a two-phase pulse having a phase difference of 90 degrees and inputs it to CPU IC Q5008 as 8-bit parallel data.

### Control Circuit

The control circuit consists of CNTL Unit IC Q5023/5025/5028-5039, etc. This circuit controls the switching of various switches, filters, transmit/receive mode, VCO, and bands and the input of signals.

### Serial Data Communication Circuit

Data transfer to PLL IC, DDS-PLL, SUB, CAR, RX2-PLL, RX2-CAR Unit, indicators, keyer, DSP, etc. is performed by 3-wire system clock synchronous communication, whereas internal ANT tuner and CAT serial signals are transferred by 2-wire system asynchronous communications.

Various types of data, such as operating frequency, mode, and display, are processed by CPU IC Q5008 and transferred as serial signals to the appropriate devices by IC Q5013 / Q5018 / Q5020 / Q5021 /Q5037.

The CAT signal is converted to RS232 interface standard levels by IC Q5006 and output from connector J5007 of D-SUB pin 9.

### Key Matrix Circuit

The key matrix circuit consists of DISPLAY Unit IC Q5506/Q5507, D5503-D5517, and panel key switches arranged on the matrix. When a key is pressed, this circuit reads the input data for processing by the CPU.

### Analog-Digital Converter Circuit

Forward and reflected-wave voltage, ALC, power supply, S-meter, COMP meter, IF SHIFT/WIDTH VR, DSP switch, PITCH VR, shuttle jog , REMOTE terminal, etc. are selected by CNTL Unit IC Q5009/5010/5038 and input to the A/D port of CPU IC Q5008 for conversion into digital values to be processed.

The individual voltages converted into digital values are displayed as PO, SWR, ALC, IC, VCC, and S-meter indications on the LCD panel. Depending on the conditions of digitally-converted VRs, switches, etc., necessary control is effected.

### LED Drive Circuit

The LED drive circuit consists of KEY Unit IC Q9501-Q9503 and LEDs. This circuit converts serial data from the CPU into parallel data and drives (turns on/off) the appropriate LEDs.

### LCD Circuit

Data processed by the CPU IC is serially input to LCD driver IC Q5501-Q5504 of the DISPLAY Unit to drive LCD display DS5501. A cold cathode tube and exclusive DC-DC inverter unit are used for back lighting of the LCD. The inverter unit supply voltage is controlled by a dimmer circuit.

### CTCSS Tone Generator Circuit

The CTCSS tone generator circuit consists mainly of CPU IC Q5008 and active filter IC Q5043-1. The tone generated by this circuit is input to the frequency modulator from connector J5011.

### Electronic Keyer Circuit

The electronic keyer circuit consists mainly of CNTL Unit IC Q5035/Q5031/Q5040 and speed control VR9362 (SPEED). When the CW mode is selected, this circuit controls the transmission operation. The key input from the keyer is connected to keyer IC from key jacks J9442-1/J5027, and its control signal is input to Q5019/Q5042/Q5041 for keying control in the CW mode.

Notes: